


# AMD AM4

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MS-7B85 BOM List



Schematic Cfg	ERP NO.	Remark	BOM
CFG-7B85-10-Performance Gaming	601-7B85-A01		A
CFG-7B85-20-Arsenal Gaming			

 <b>MICRO-START INT'L CO.,LTD.</b>	
COVER SHEET	
Size C	Document Number <b>MS-7B85</b>
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# MS-7B85

AMD

Raven Ridge

Pinnacle Ridge

95W

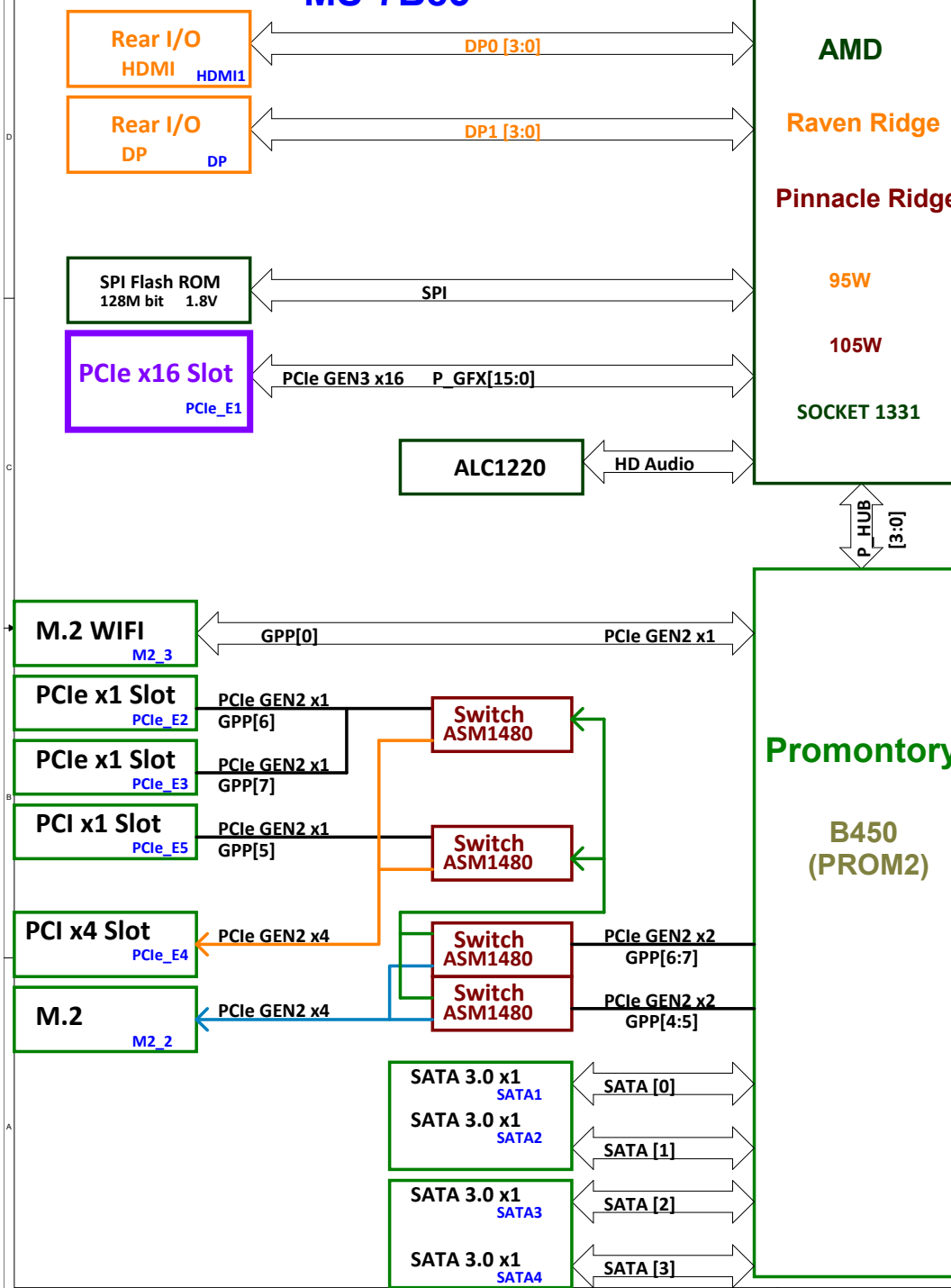
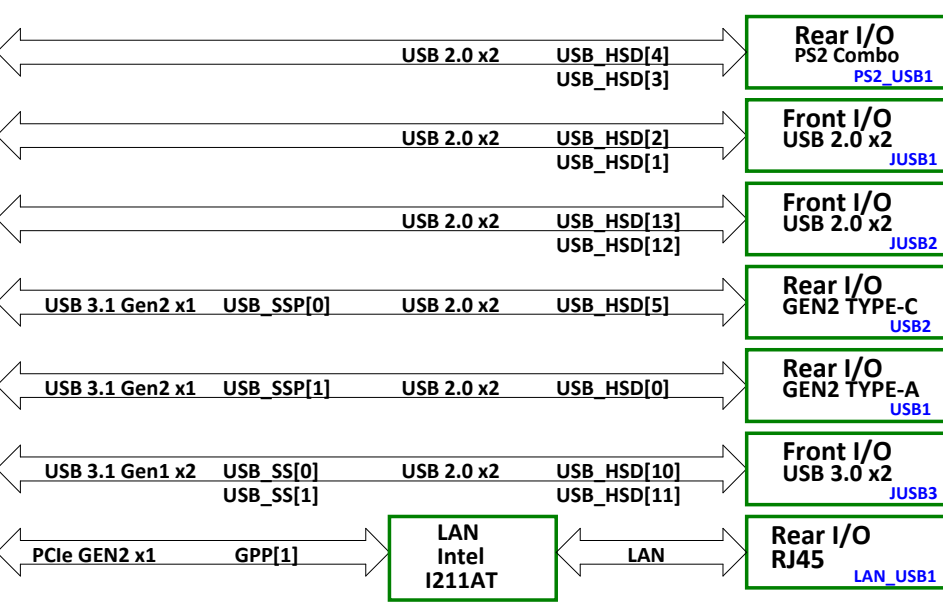
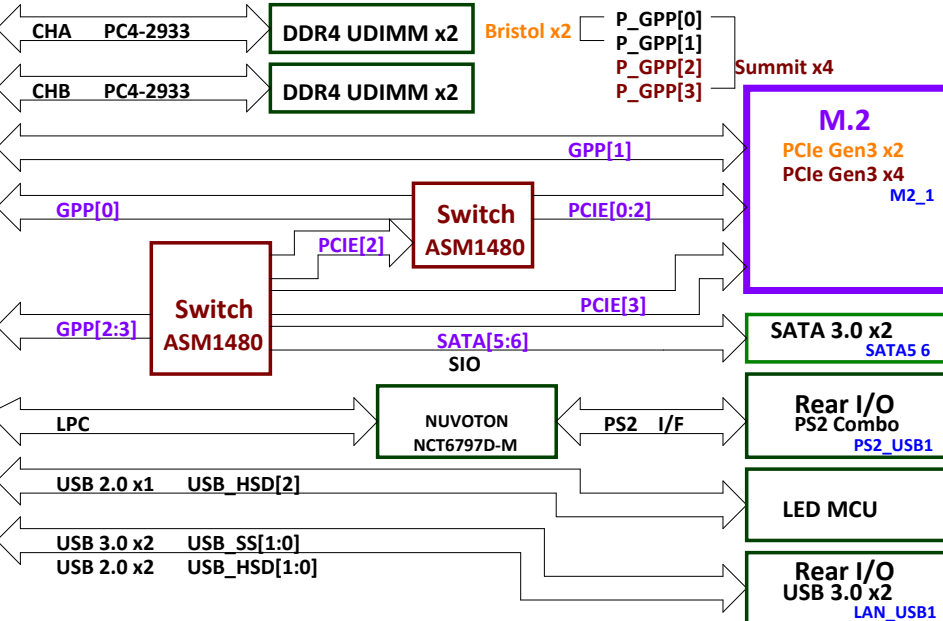
105W

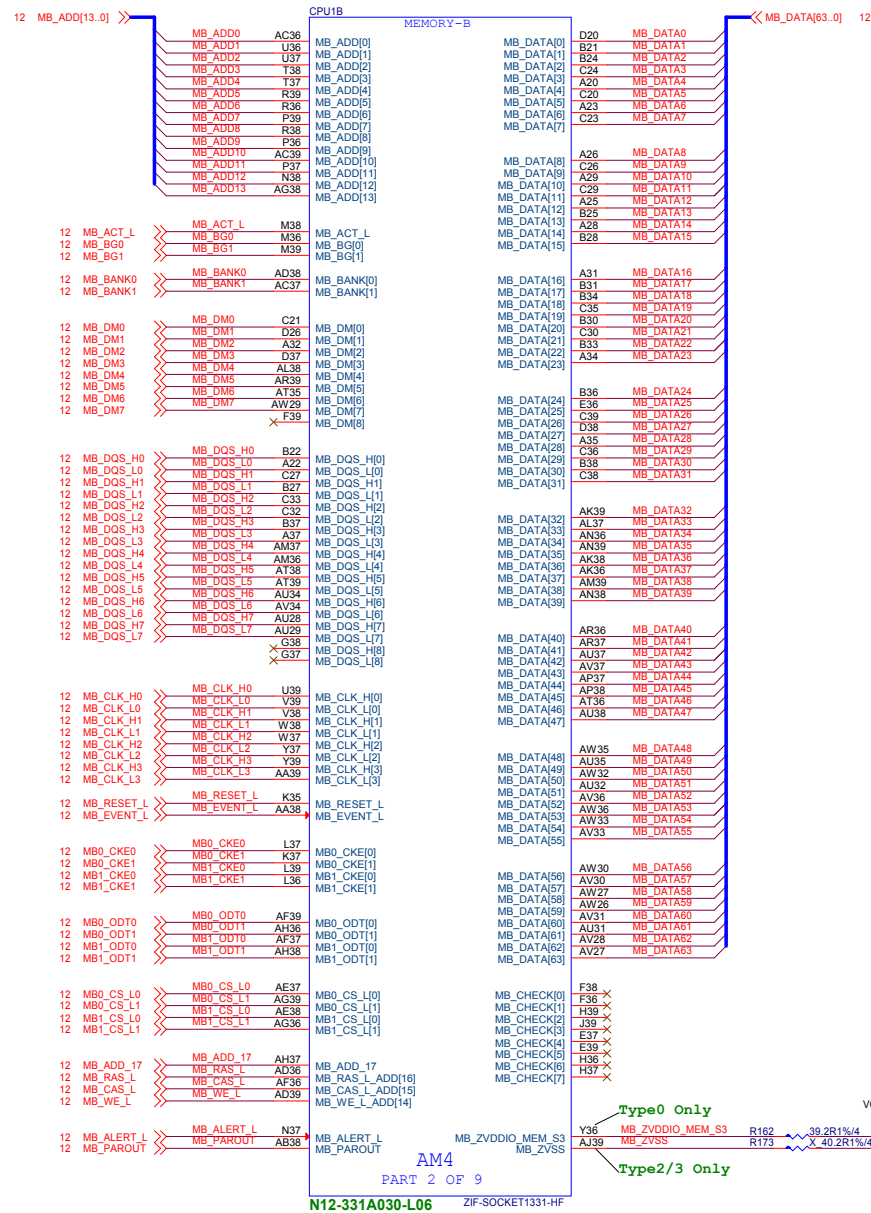
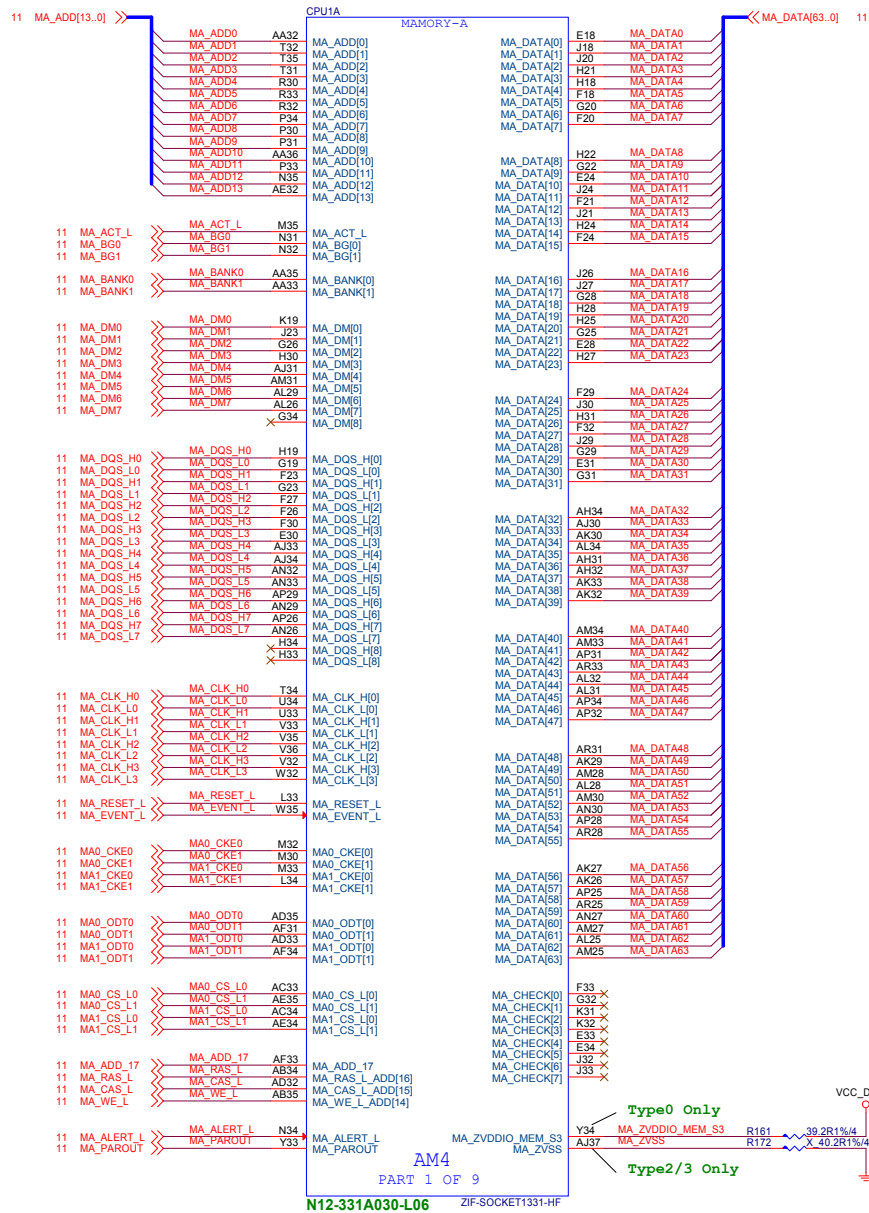
SOCKET 1331

P\_HUB  
[3:0]

Promontory

B450  
(PROM2)





Schematic Cfg		Project	
CFG-7B85-10-Performance Gaming		V	A
CFG-7B85-20-Arsenal Gaming			

**MSI**  
MICRO-START INT'L CO., LTD.

File: **AM4 DDR4 I/F**

Size: Custom Document Number: **MS-7B85** Rev: **11**

Date: Friday, June 29, 2018 Sheet 3 of 75

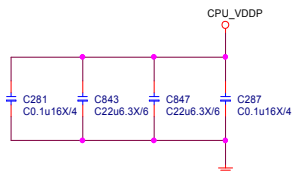
Not supported HUB on TYPE 1

Not supported PCIE on TYPE 0,1

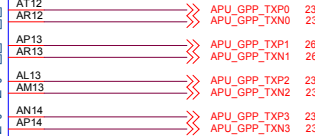
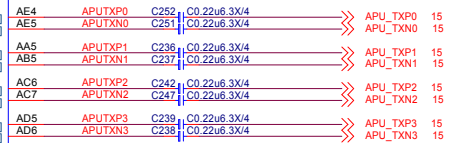
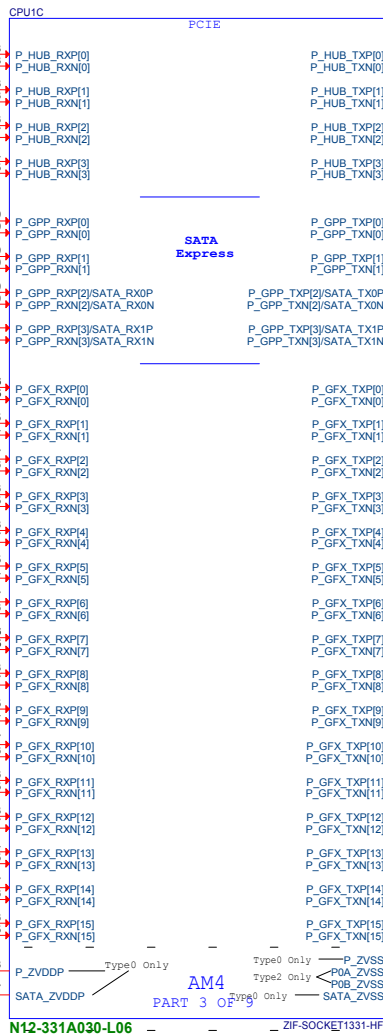
TYPE 0	PCIE	SATA
TYPE 2/3	2 or 4	2 or 0

Not supported GFX 4~15 on TYPE,1

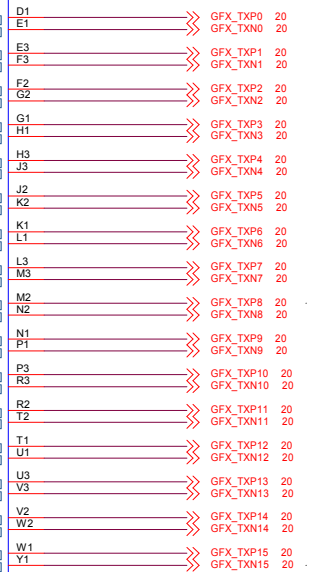
Only supported on TYPE 2  
Not supported GFX 8~15 on TYPE 0,3



Within 1500 mils from APU  
Within 1000 mils from APU




SATA5, SATA6  
Not supported PCIE on TYPE 0,1



Only supported on TYPE 2

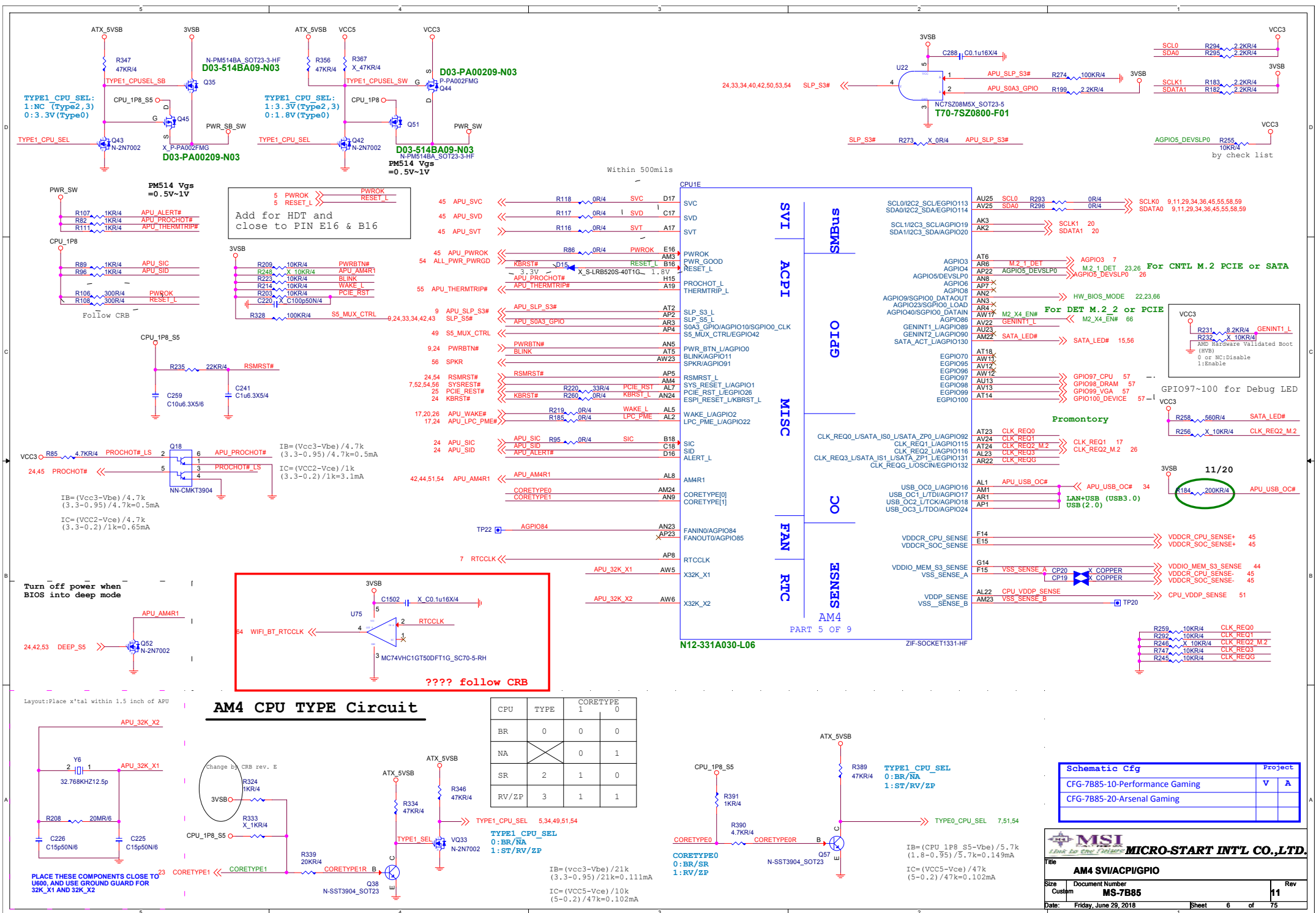
Within 1500 mils from APU  
Within 1000 mils from APU

Schematic Cfg	Project
CFG-7B85-10-Performance Gaming	V A
CFG-7B85-20-Arsenal Gaming	

**MICRO-START INT'L CO.,LTD.**

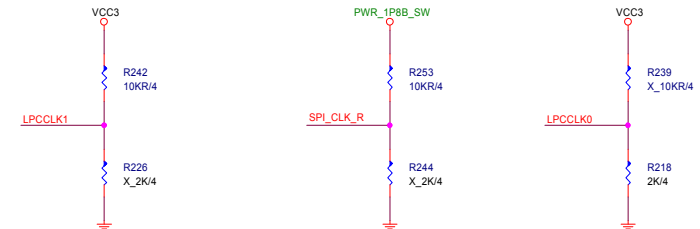
File		AM4 PCIE/SATAE	
Size	Document Number	Rev	
Custom	MS-7B85	11	
Date:	Friday, June 29, 2018	Sheet	4 of 75



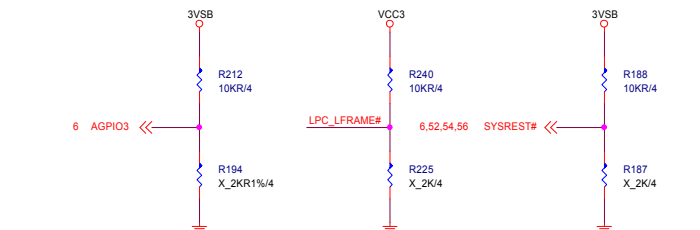




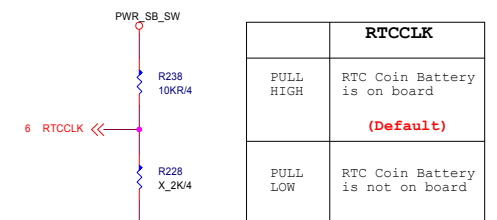
# Strapping Options



	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator <b>(Default)</b>	Use 48Mhz crystal clock and generate both internal and external clocks <b>(Default)</b>	LPC device Boot Fail Timer Enabled
PULL LOW	Configured for External clock generator ????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC device Boot Fail Timer Disabled <b>(Default)</b>



	AGPIO3	SIO_LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic <b>(Default)</b>	SPI ROM <b>(Default)</b>	Normal reset mode <b>(Default)</b>
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode



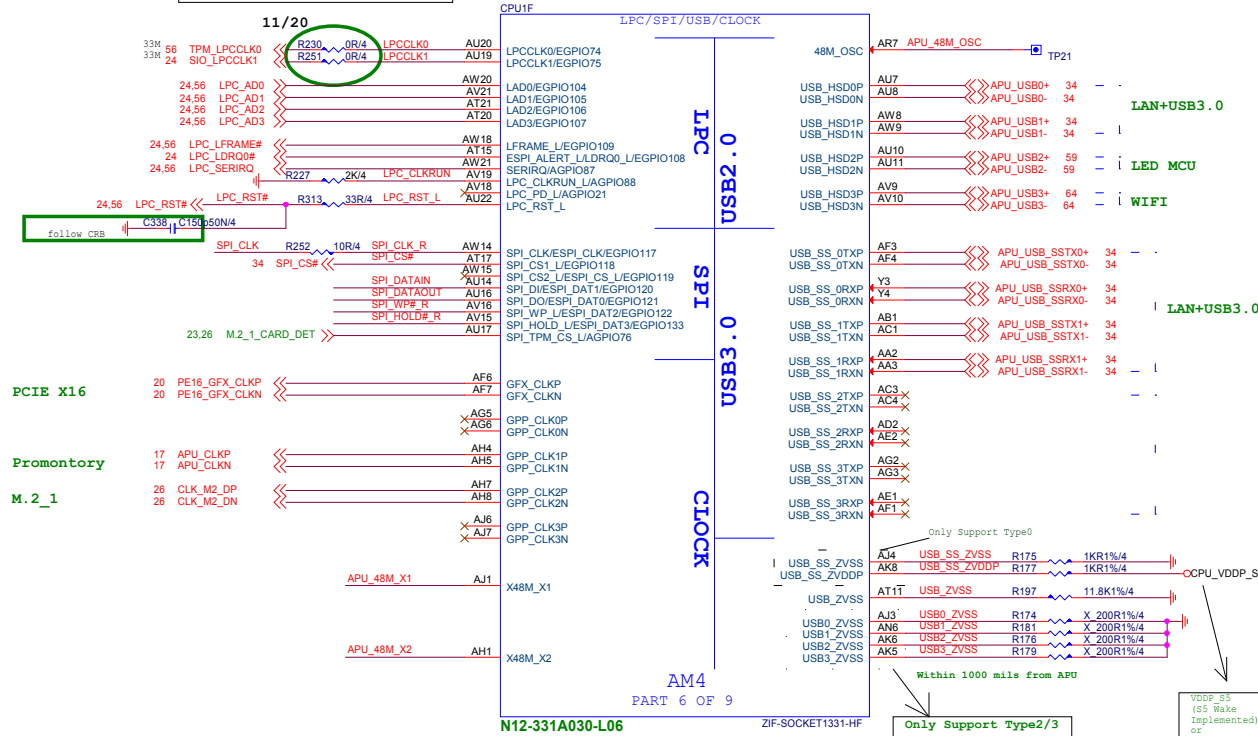
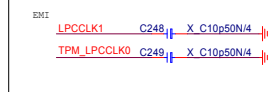
	RTCCLK
PULL HIGH	RTC Coin Battery is on board <b>(Default)</b>
PULL LOW	RTC Coin Battery is not on board

**MSI**  
MICRO-START INT'L CO.,LTD.

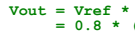
File: **AM4 LPC/SPI/USB/CLK/STRAP**

Size: Custom Document Number: **MS-7B85** Rev: **11**

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1.5V@0.25A


$$= 1.507V$$


VCORE



VCORE

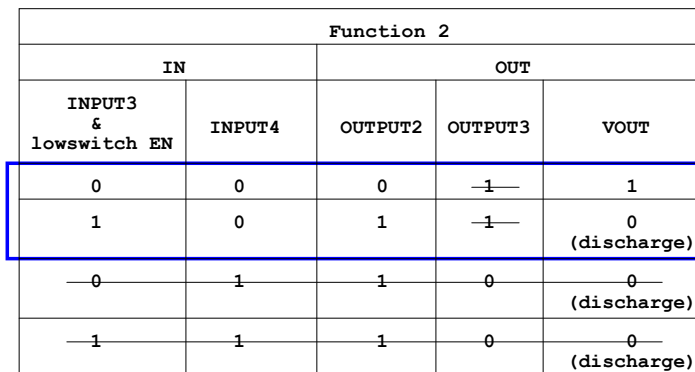
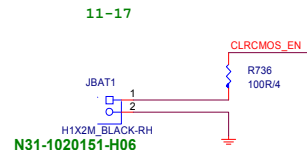
Title	08 AM4 Power/DDRIO, AUDIO Power
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Custom	MS-7B85	11
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Placement Bottom Side

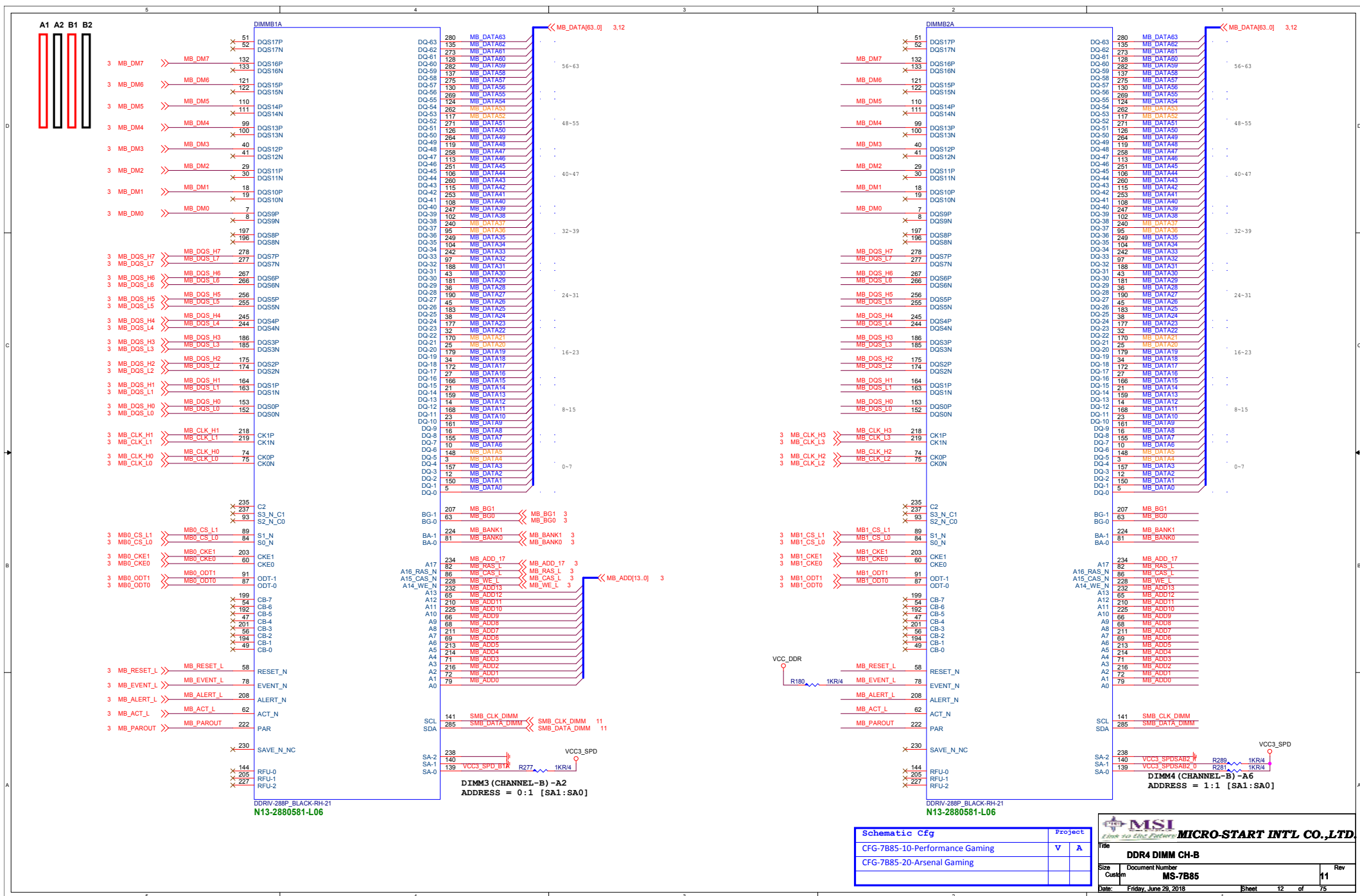


Default

GND

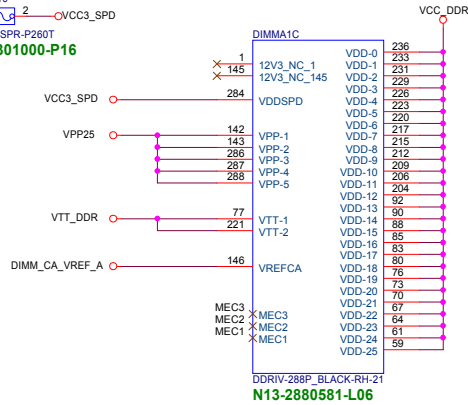
AM4  
PART 9 OF 9



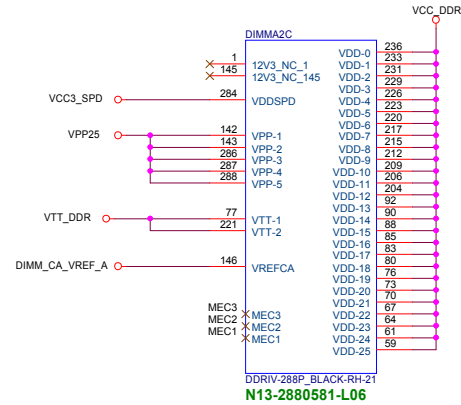


av1:D08-0301100-B07

VCC3 1 F10 2 VCC3\_SPD  
F-SPR-P260T  
D08-0301000-P16

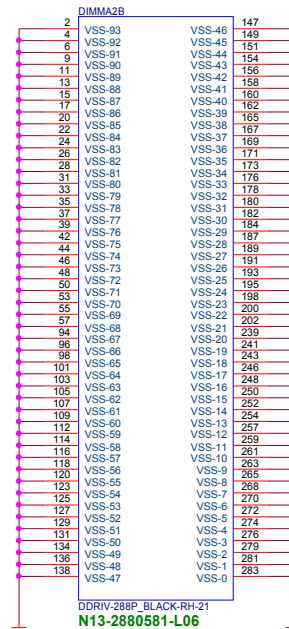
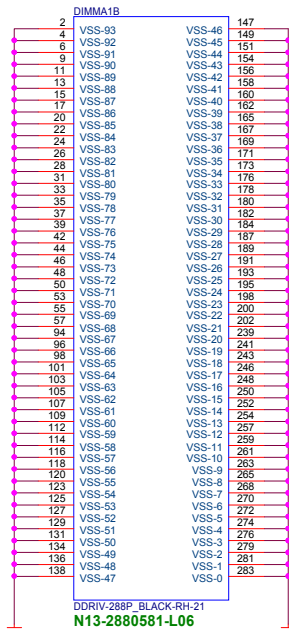
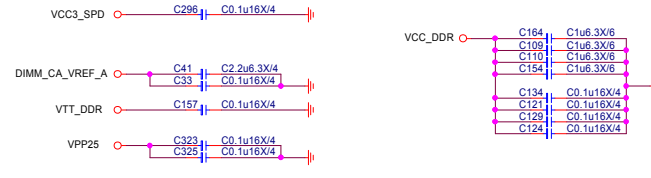
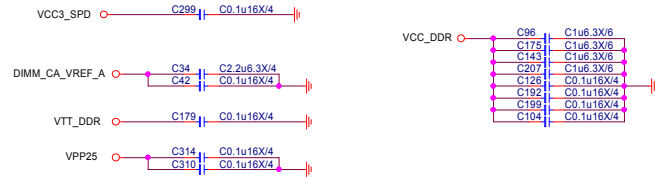
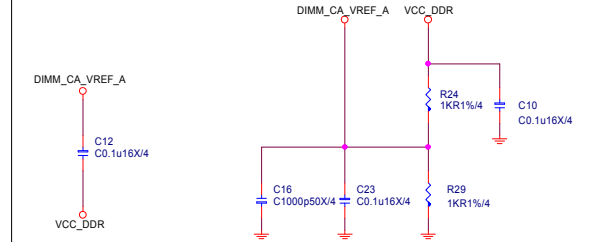


DIMM SLOT PN BY SPEC



## DDR VREF

(place resistors close to DIMMs)



5

4

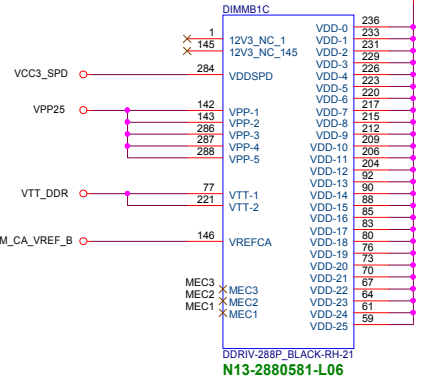
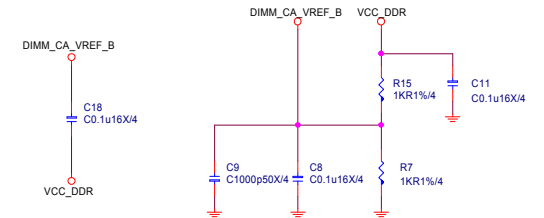
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2

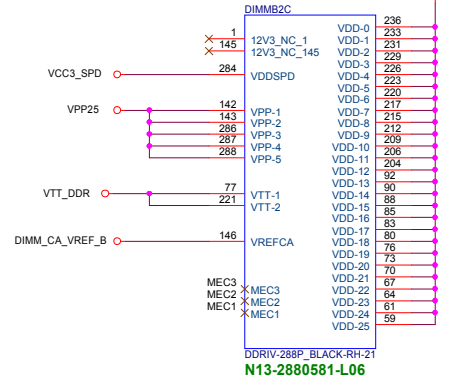
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## DDR VREF

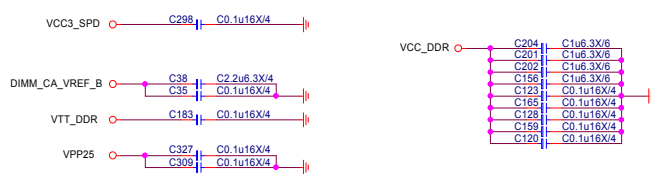
(place resistors close to DIMMs)



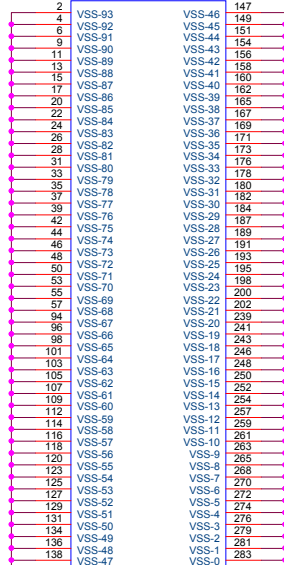
DDRIV-288P\_BLACK-RH-Z1  
N13-2880581-L06



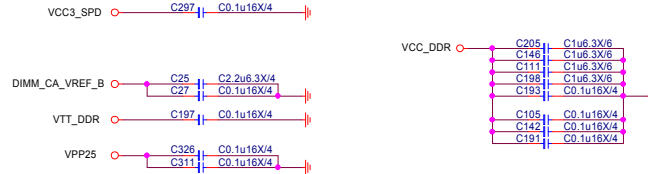
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N13-2880581-L06



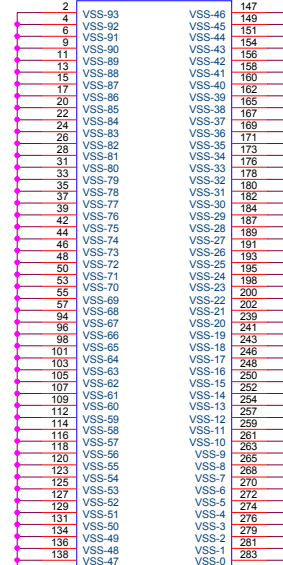
DIMMB1B



DDRIV-288P\_BLACK-RH-Z1  
N13-2880581-L06

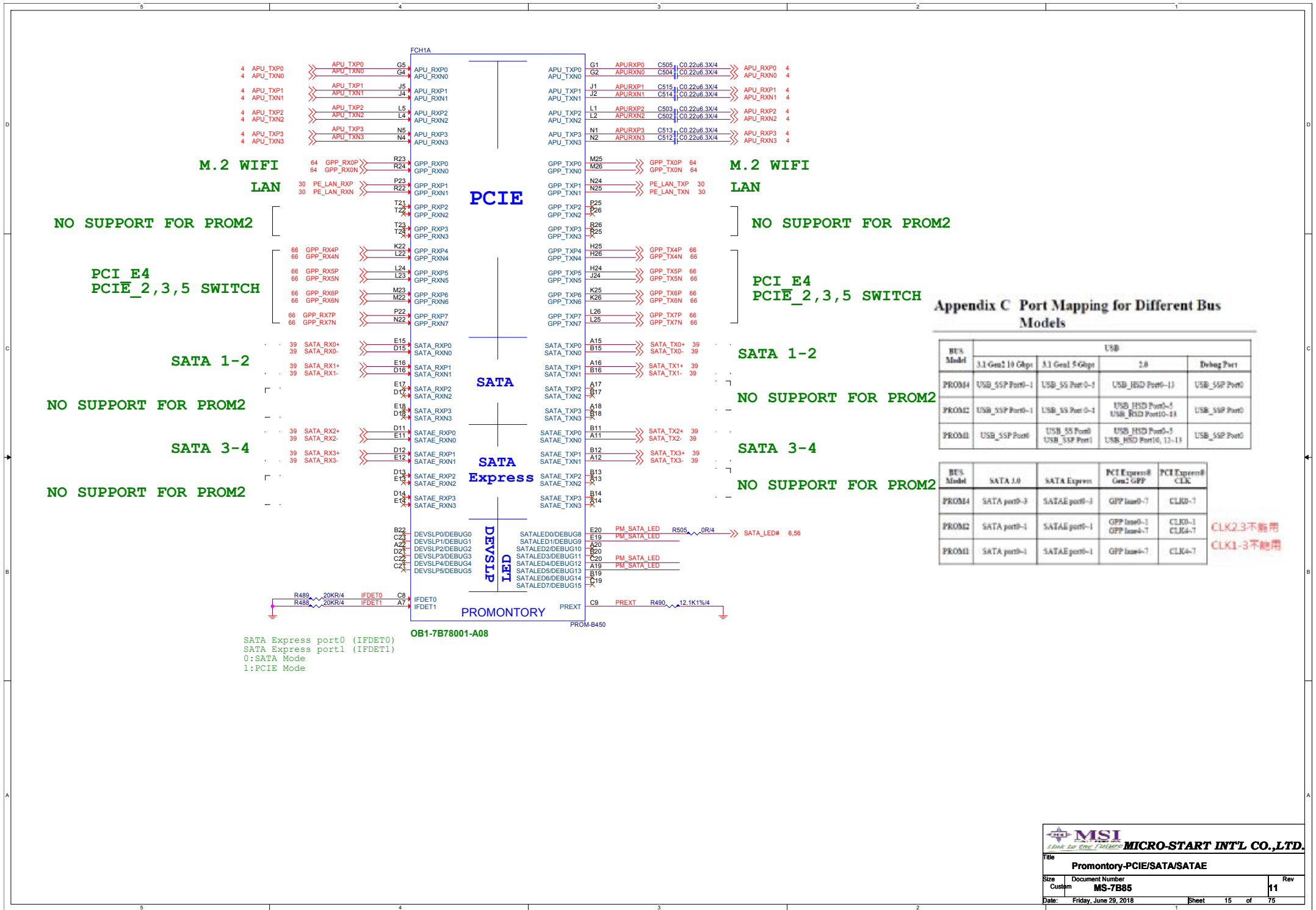


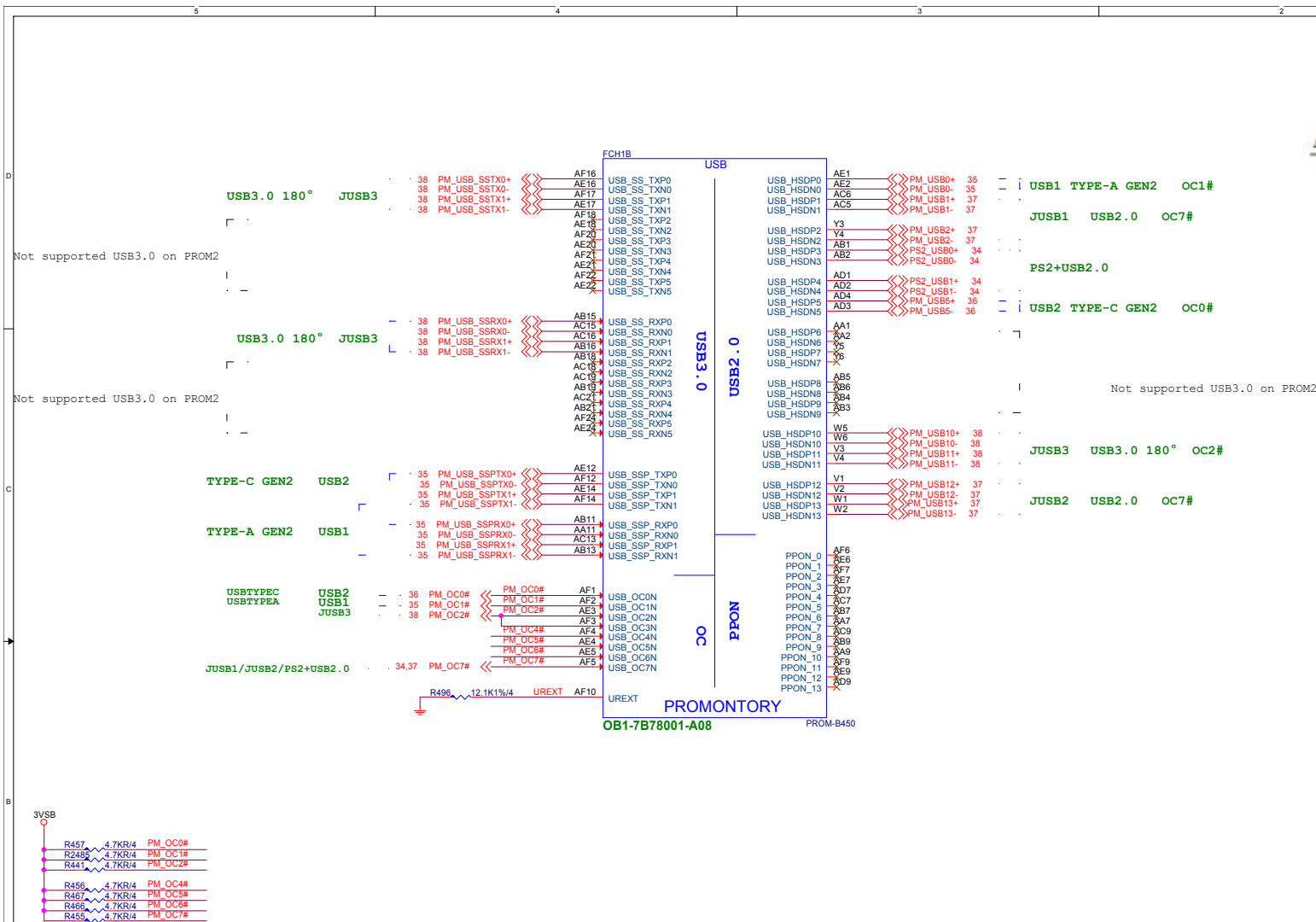
DIMMB2B



DDRIV-288P\_BLACK-RH-Z1  
N13-2880581-L06







## Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP[N]0	USB_HSDP[N]5	USB_OC0N
USB_SSP_TX/RXP[N]1	USB_HSDP[N]0	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SSP_TX/RXP[N]0	USB_HSDP[N]10	USB_OC0N
USB_SSP_TX/RXP[N]1	USB_HSDP[N]11	USB_OC0N
USB_SSP_TX/RXP[N]2	USB_HSDP[N]6	USB_OC4N
USB_SSP_TX/RXP[N]3	USB_HSDP[N]7	USB_OC3N
USB_SSP_TX/RXP[N]4	USB_HSDP[N]8	USB_OC6N
USB_SSP_TX/RXP[N]5	USB_HSDP[N]9	USB_OC7N
	USB_HSDP[N]1	USB_OC7N
	USB_HSDP[N]2	USB_OC7N
	USB_HSDP[N]3	USB_OC7N
	USB_HSDP[N]4	USB_OC7N
	USB_HSDP[N]12	USB_OC7N
	USB_HSDP[N]13	USB_OC7N

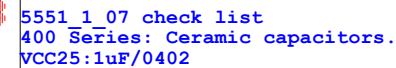
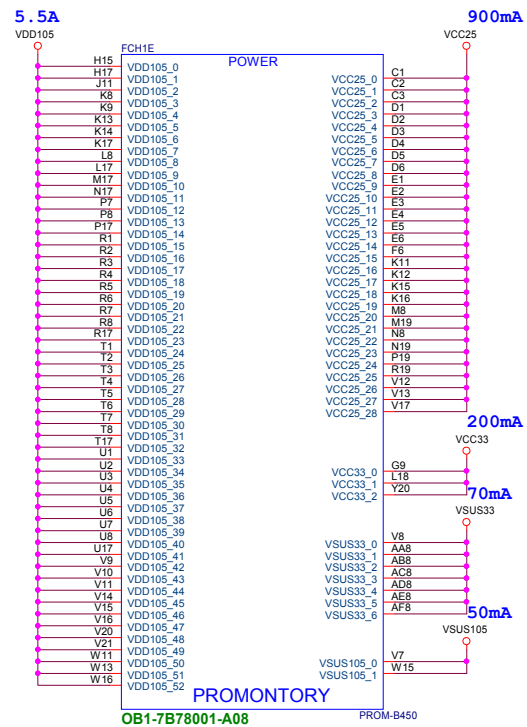
## Appendix C Port Mapping for Different Bus Models

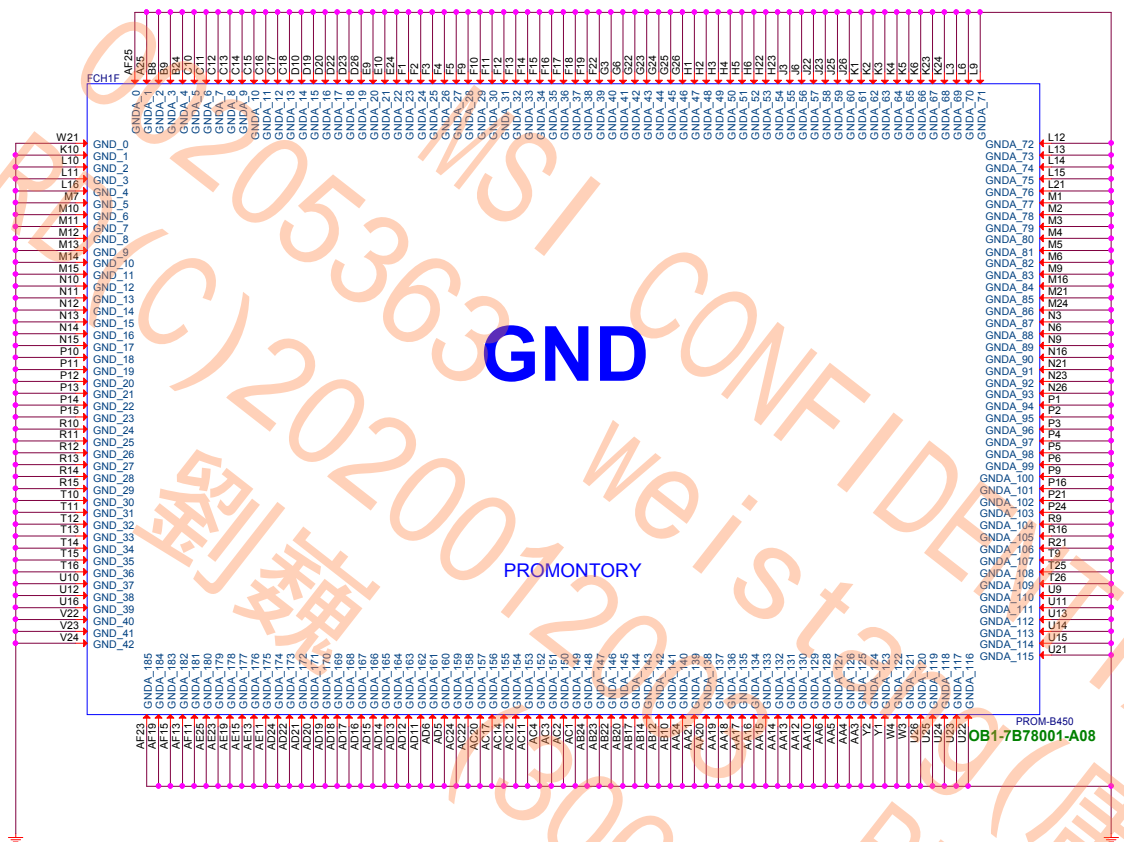
BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM14	USB_SSP Port0-1	USB_SSP Port0-1	USB_HSD Port0-13	USB_SSP Port0
PROM12	USB_SSP Port0-1	USB_SSP Port0-1	USB_HSD Port0-5 USB_HSD Port10-13	USB_SSP Port0
PROM11	USB_SSP Port0	USB_SSP Port0	USB_HSD Port0-5 USB_HSD Port10, 12-13	USB_SSP Port0

BUS Model	SATA J.0	SATA Express	PCI Express® Gen1 GPP	PCI Express® CLK
PROM14	SATA port0-3	SATAE port0-3	GPP lane0-7	CLK0-7
PROM12	SATA port0-1	SATAE port0-1	GPP lane0-3 GPP lane4-7	CLK0-1 CLK4-7
PROM11	SATA port0-1	SATAE port0-1	GPP lane0-7	CLK4-7

CLK2,3不能  
CLK1-3不能

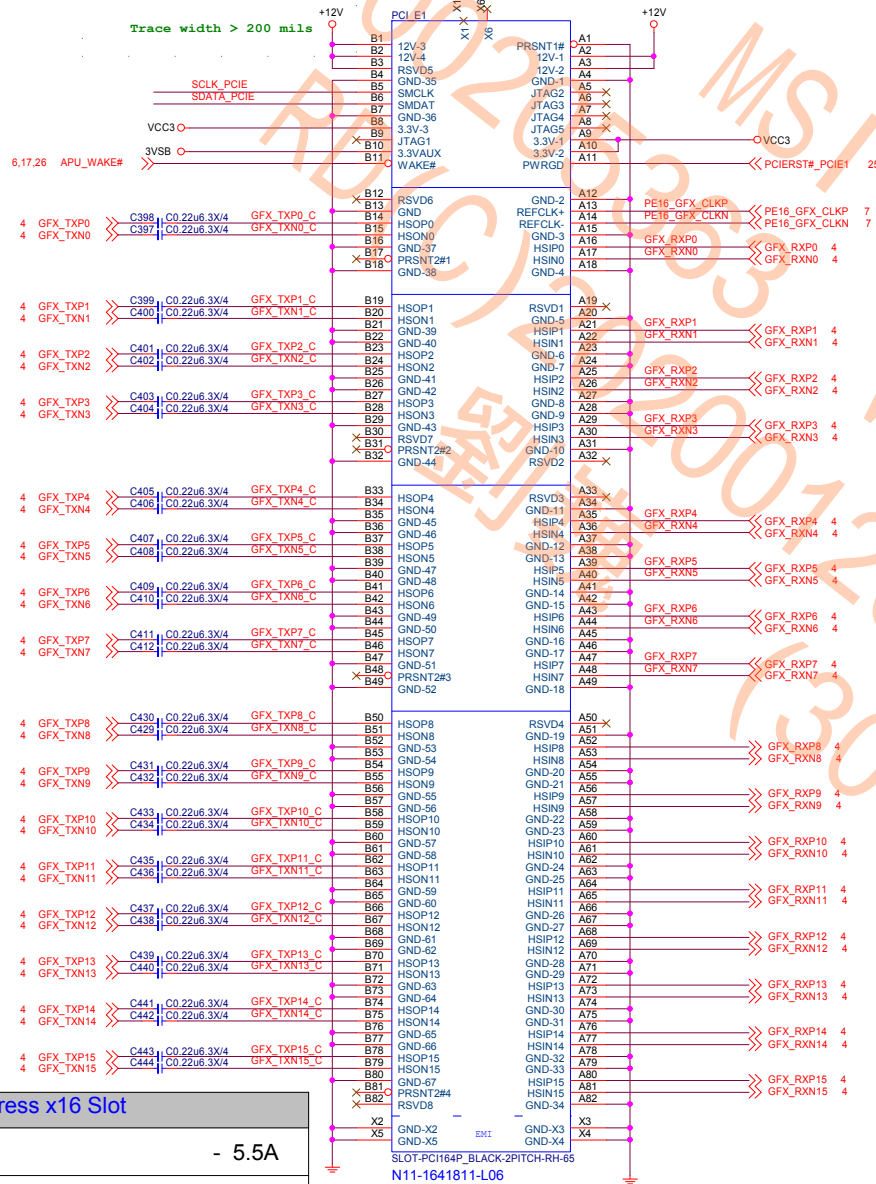






# PCI EXPRESS x16 Slot

## PCI\_E1






PCI\_E2

```

20 SCLK_PCIE >>>
20 SDATA_PCIE >>>
VCC3 >
3VSB >
17,21,30,64,65 PM_WAKE# <<<

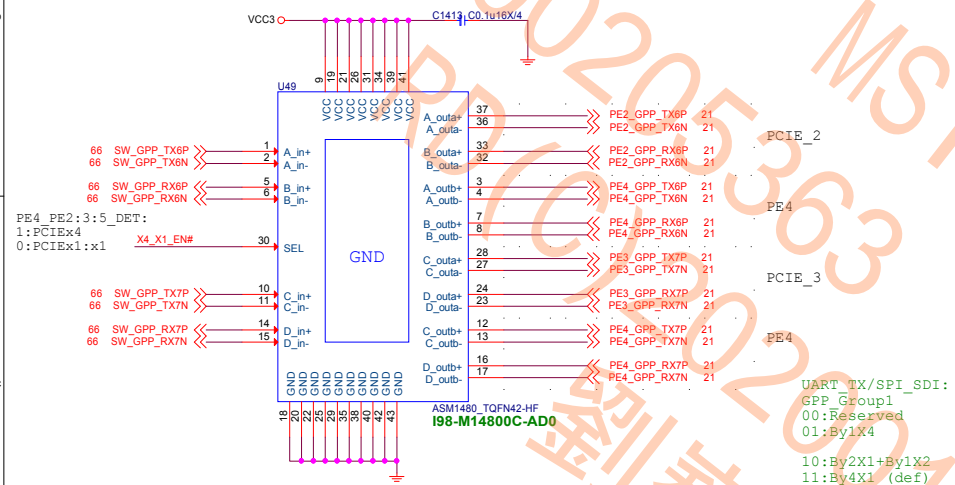
```



 <b>MSI</b> <i>Link to the Future</i>				<b>MICRO-START INT'L CO.,LTD.</b>			
Title							
<b>PCI_E2_E3_E5/E4 X1/X4</b>							
Size		Document Number				Rev	
Custom		<b>MS-7B85</b>				<b>11</b>	
Date:		Friday, June 29, 2018		Sheet		21 of 75	

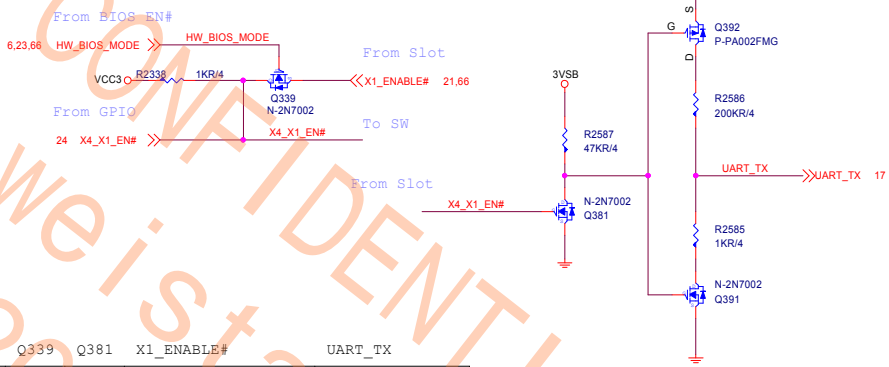
Schematic Cfg	Project	
CFG-7B85-10-Performance Gaming	V	A
CFG-7B85-20-Arsenal Gaming		

PCI\_E4 and PCIE\_2 :3 :5 Switch

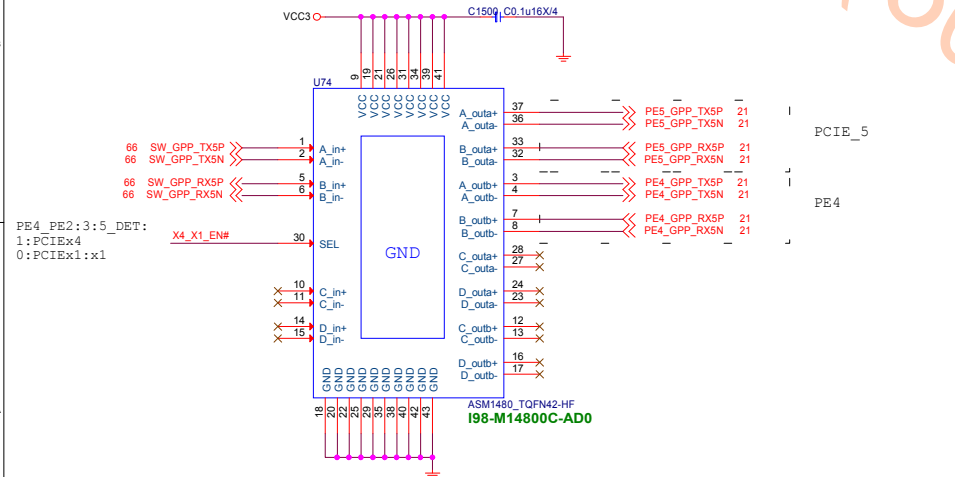


SEL	Function
L	N_in +/1 to N_outa+/-
H	N_in +/1 to N_outb+/-

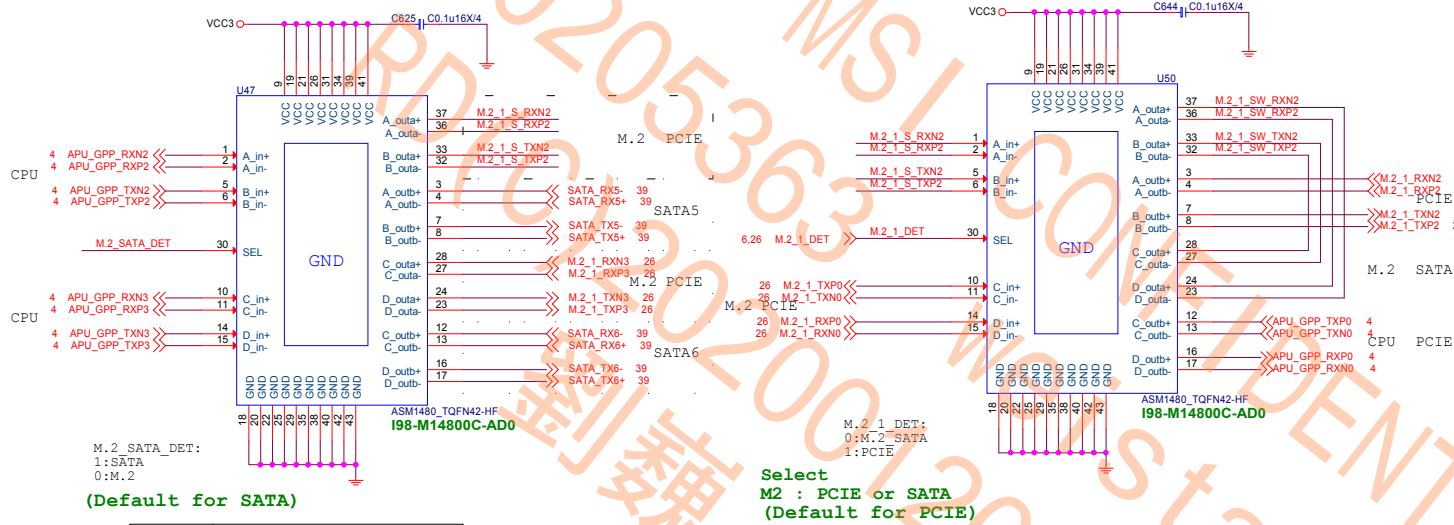
PCIE Lanes control circuit



	HW_BIOS_MODE	Q339	Q381	X1_ENABLE#	UART_TX
Manual x4	L	OFF	OFF	X	11:By4x1 (def)
Manual x1,x1,x1,x1	L	OFF	OFF	L	01:By1X4
HW x4	H	ON	ON	H	11:By4X1 (def)
H/W x1,x1,x1,x1	H	ON	ON	L (Stuff PCIE_2.3.5)	01:By1X4



M2\_1 and SATA5 6 Switch

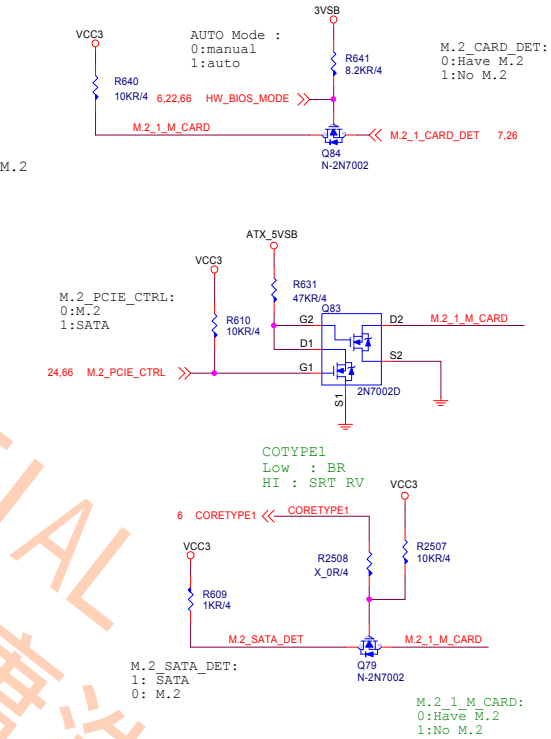


M.2 SATA\_DET:  
1:SATA  
0:M.2  
(Default for SATA)

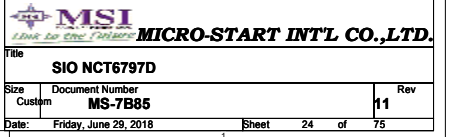
SEL	Function
L	N_in +/1 to N_outa+/-
H	N_in +/1 to N_outb+/-

Select  
M2 : PCIE or SATA  
(Default for PCIE)

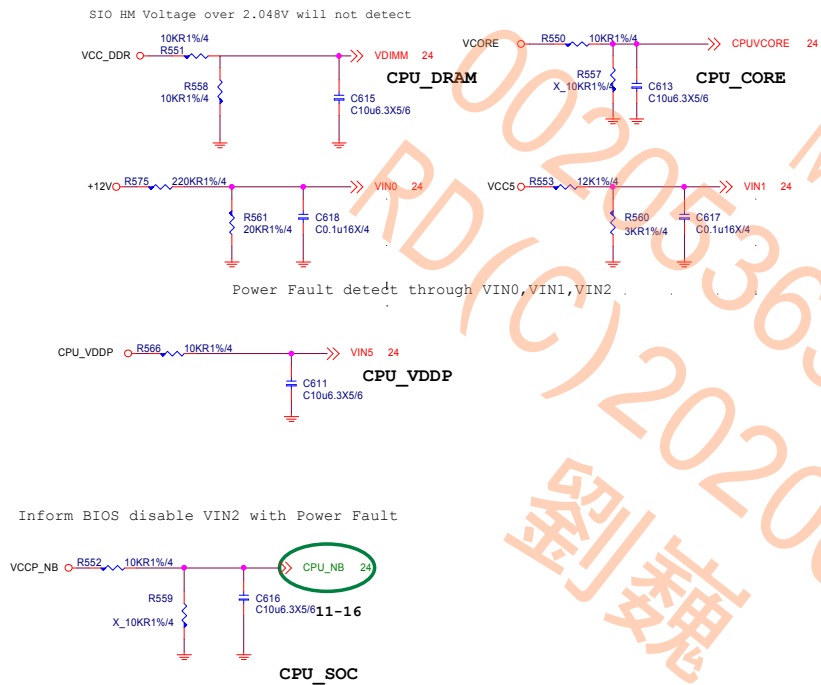
	AUTO Mode	SATA CON	M.2 (PCIE)	M.2 (SATA)
HW_BIOS_MODE	1		0	0
M.2_PCIE_CTRL	1		0	0
M.2_1_CARD_DET		1	0	0
M.2_DET		X	1	0



CPU	TYPE	CORETYPE1	
		1	0
BR	0	0	0
NA	0	0	1
SR	2	1	0
RV/ZP	3	1	1

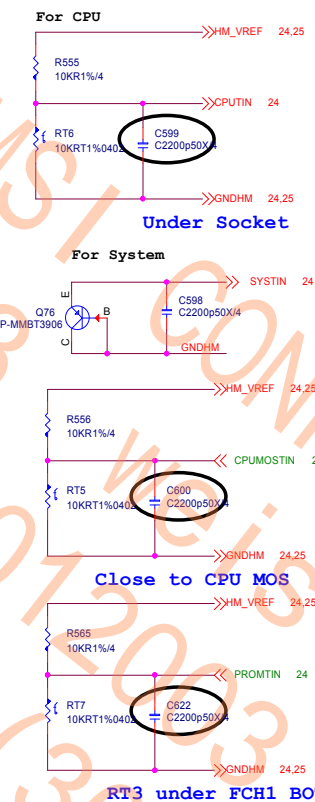


## HW Monitor - Voltage

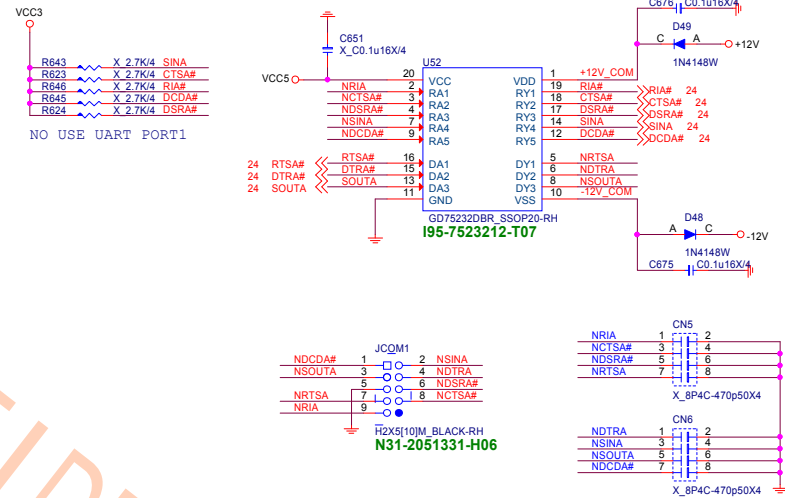


## PARALLAL PORT

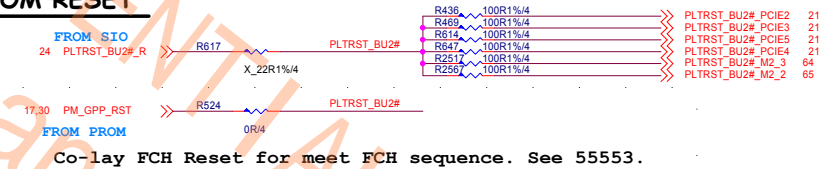
## TEMP SENSOR



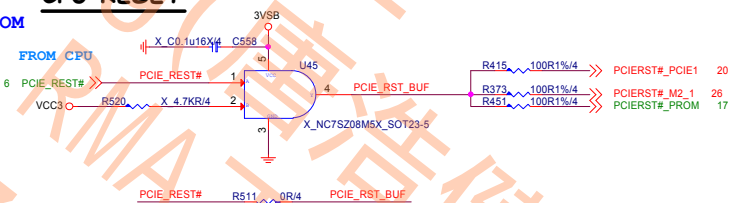
**COM PORT**



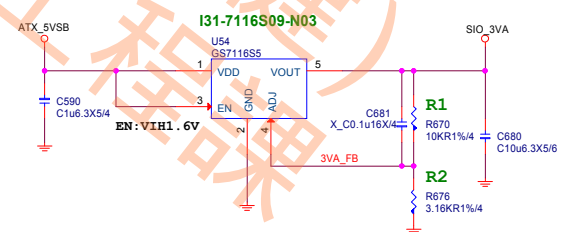
PROM RESET



## CPU RESET



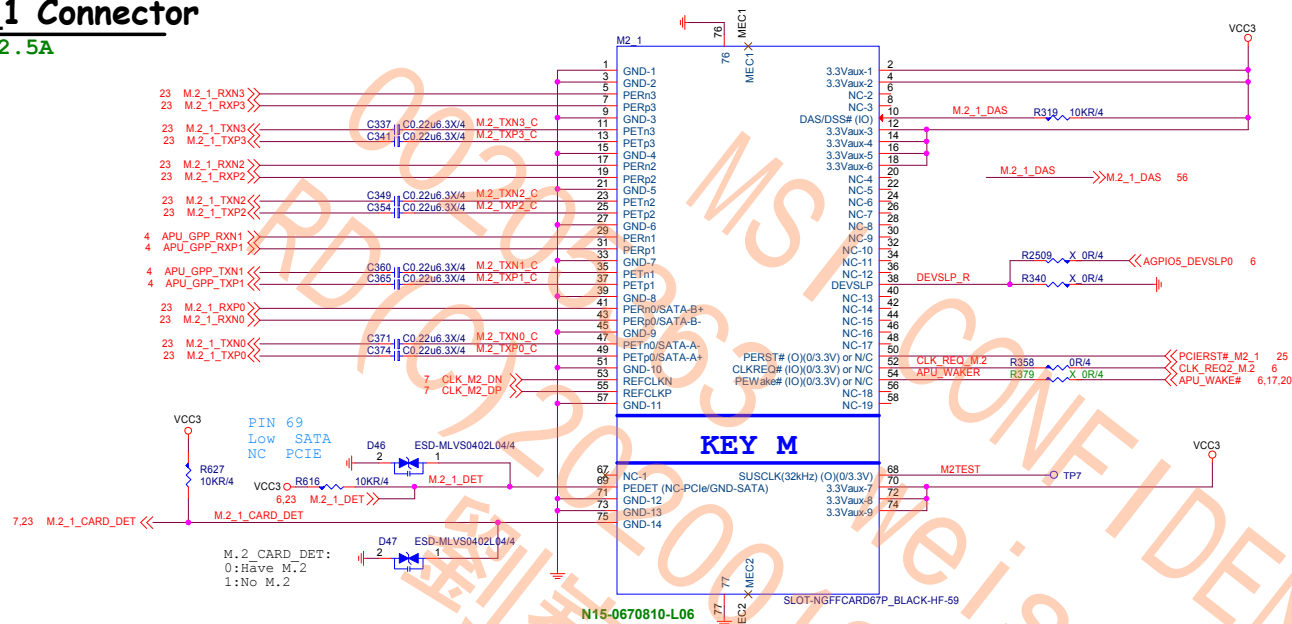
**SIO\_3VA**



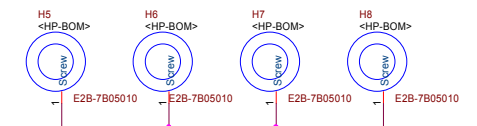
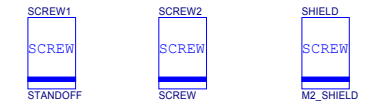
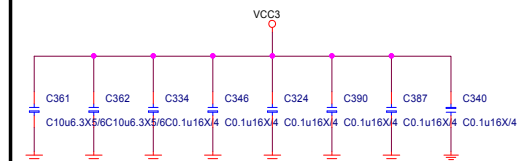
$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (10K/3.16K)) \\ &= 3.33V \end{aligned}$$

## M.2\_1 Connector

3.3V@2.5A



3.3V@2.5A



Footprint: H\_R240D173\_BR189\_PT  
E2B-7B05010-A89 E2B-7B05010-A89 E2B-7B05010-A89 E2B-7B05010-A89

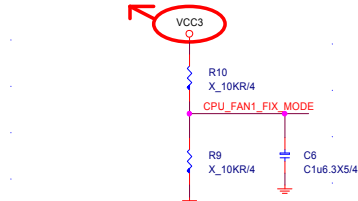
Schematic Cfg	Project
CFG-7B85-10-Performance Gaming	V A
CFG-7B85-20-Arsenal Gaming	

MSI	MICRO-START INT'L CO.,LTD.
File	M.2_1
Size	Custom
Document Number	MS-7B85
Date	Friday, June 29, 2018
Sheet	26 of 75
Rev	11

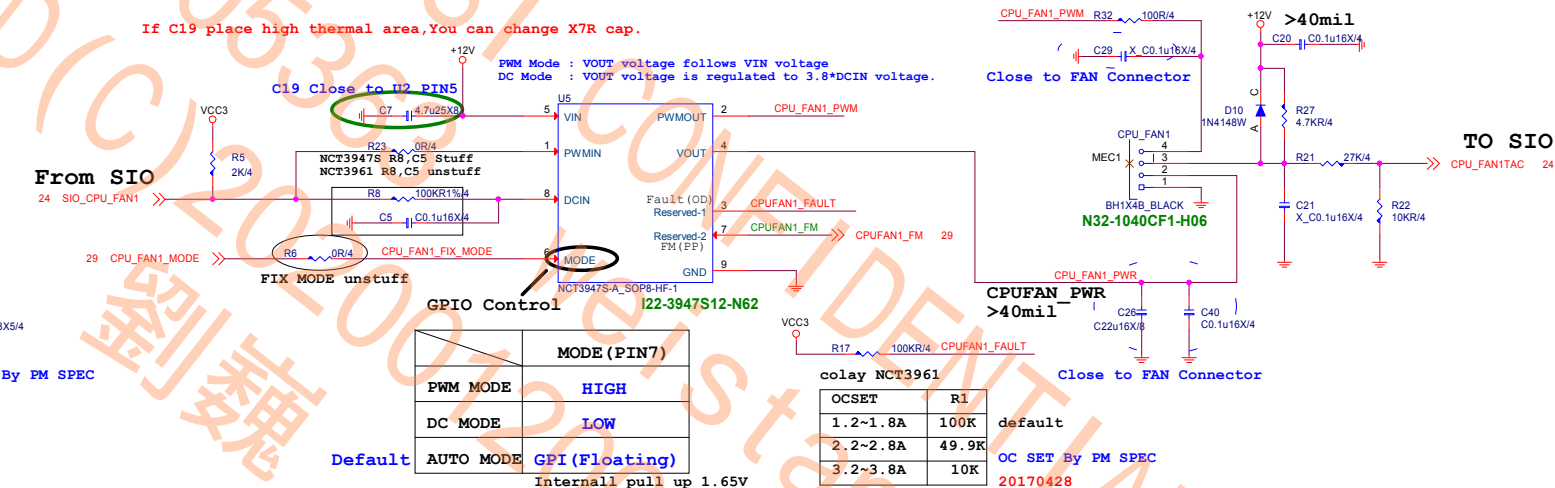


- 1.Mode GPIO BIOS can swtich PWM/DC MODE
- 2.FM:BIOS can read FAN PWM/DC MODE

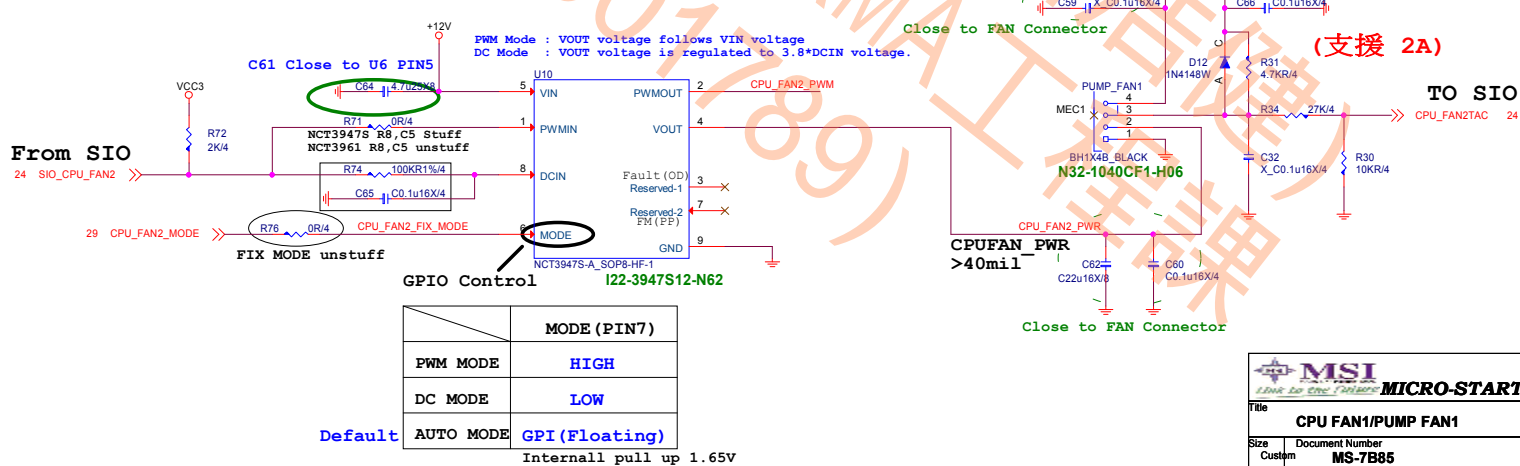
- **Avoid NCT3947S MODE PIN Leakage**



Resever For FIX DC or PWM MODE USE By PM SPEC

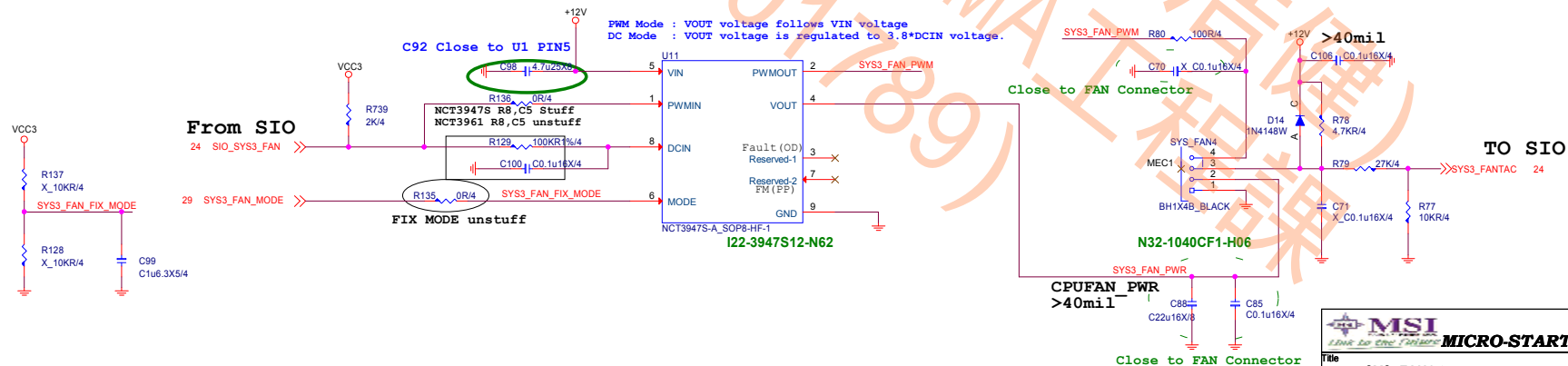
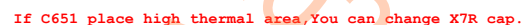


If C61 place high thermal area, You can change X7R cap.



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

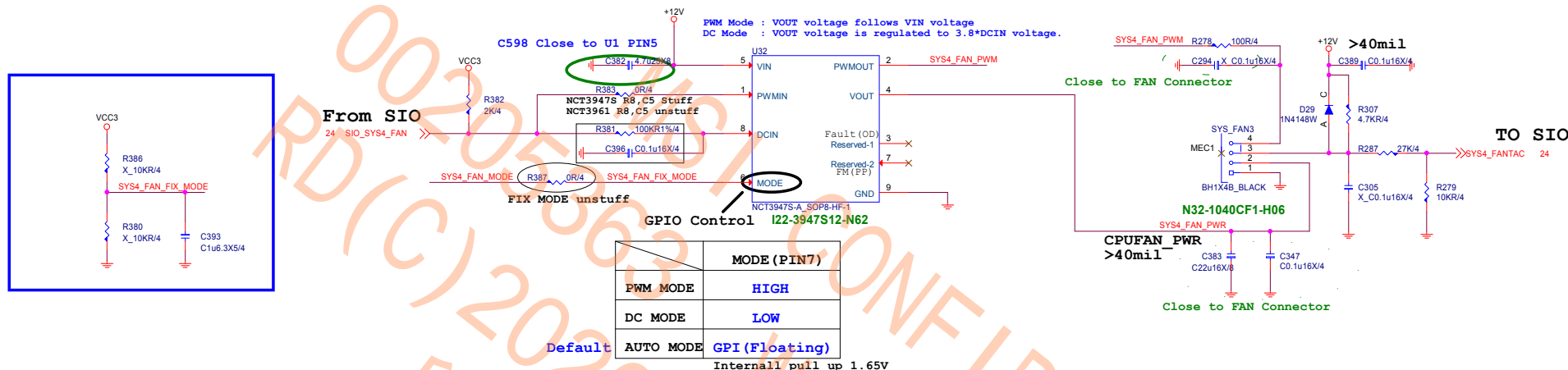
If C291 place high thermal area, You can change X7R cap.  
C291 Close to U24-PTN5



# SYSFAN 4

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

If C598 place high thermal area, You can change X7R cap.



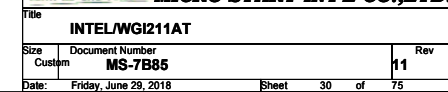
## 1. GENERAL DESCRIPTION

The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPI/O pins. It also can provide SMBus™ address setting pins to set the address during power- on reset or from external reset.

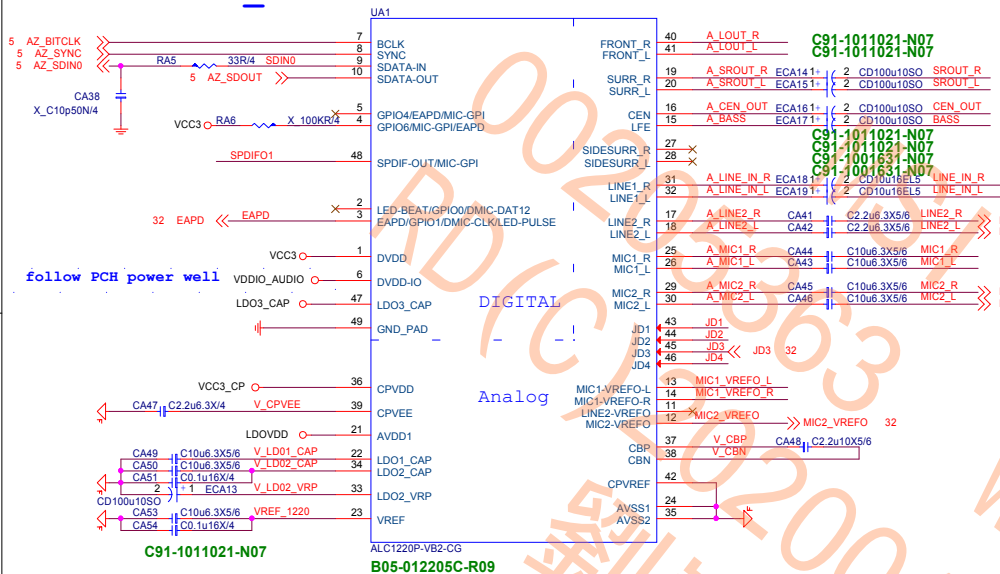
NCT5605Y SMBus™ Address is:

0	0	1	1	A2	A1	A0	R/W
---	---	---	---	----	----	----	-----

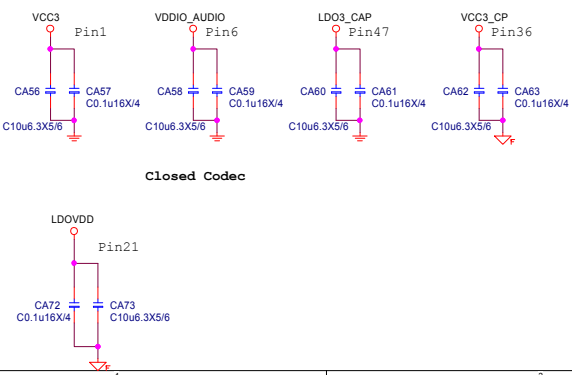
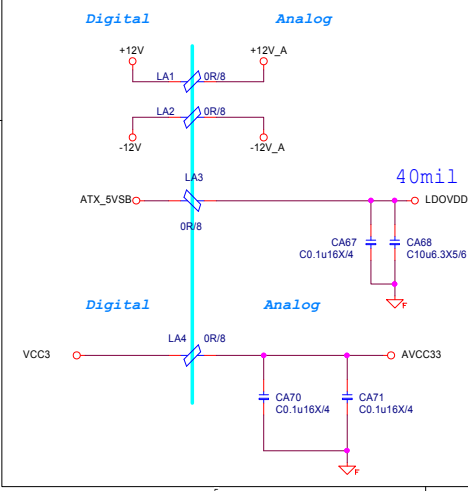
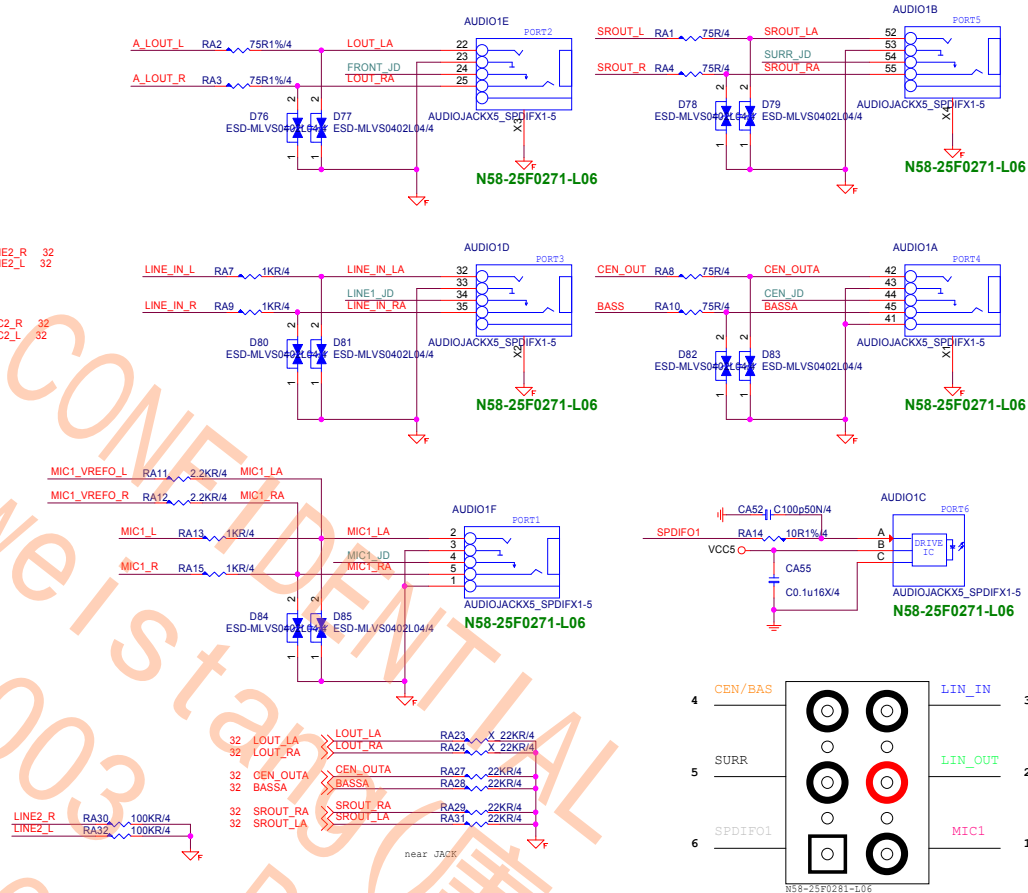
i211



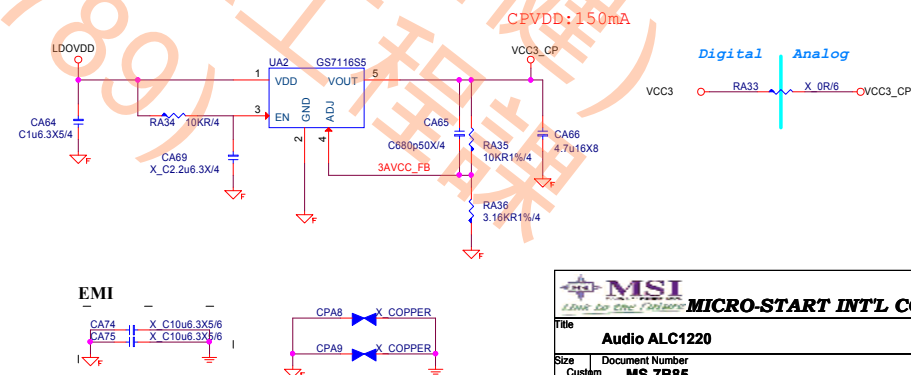
## ALC1220P-VB1 48PIN



all of JD resistors should be placed  
as close as possible to the sense pin of codec.

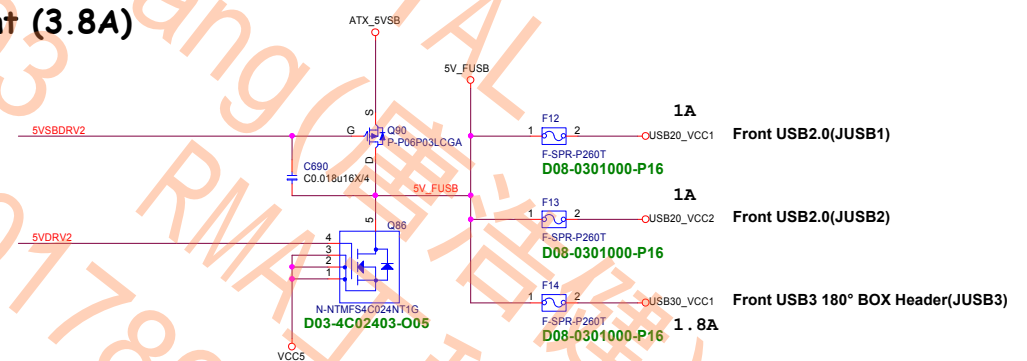
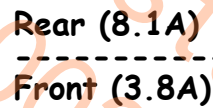


CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V

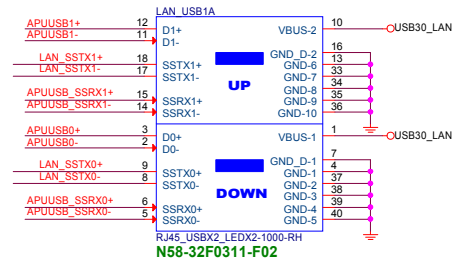
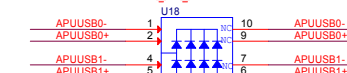
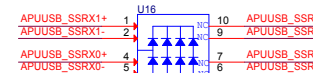
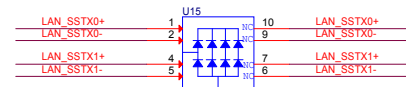
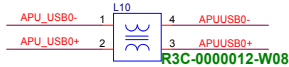




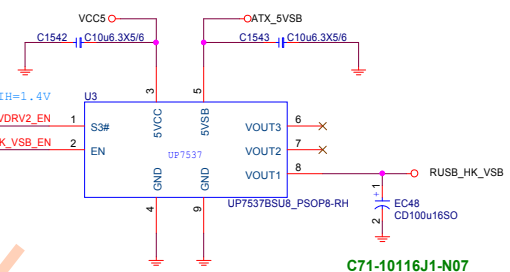
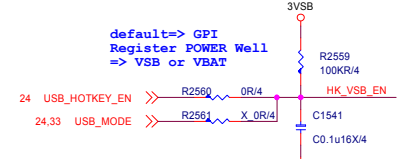
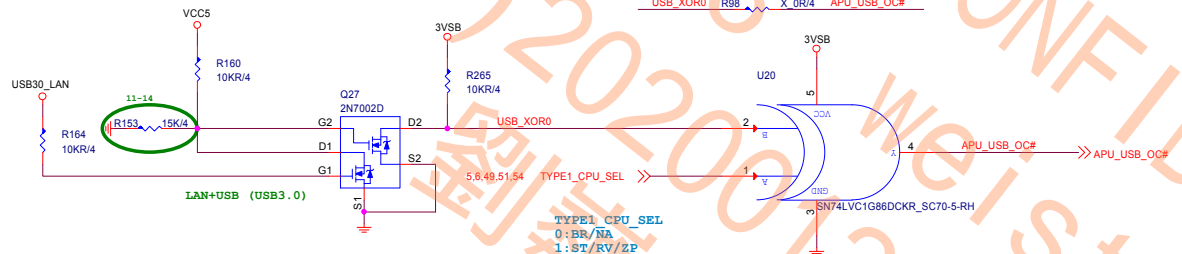


[illegible]

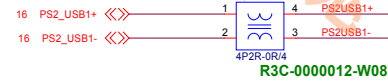
5V@1A



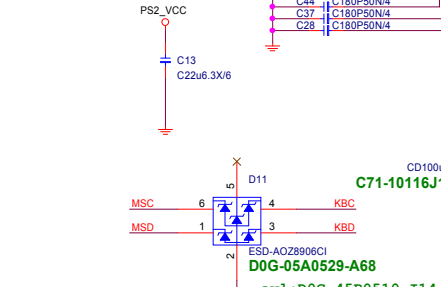
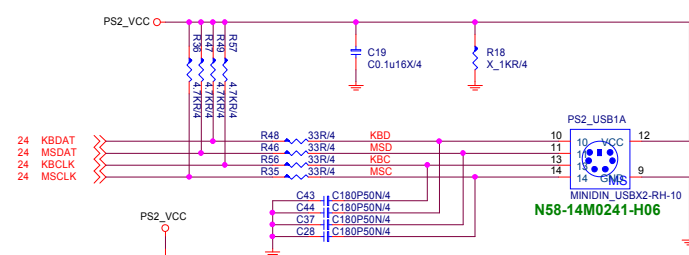
## VCC5



## 5V@1A

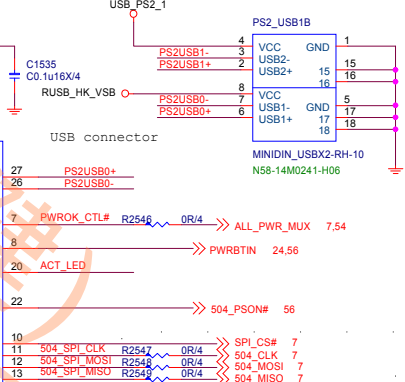
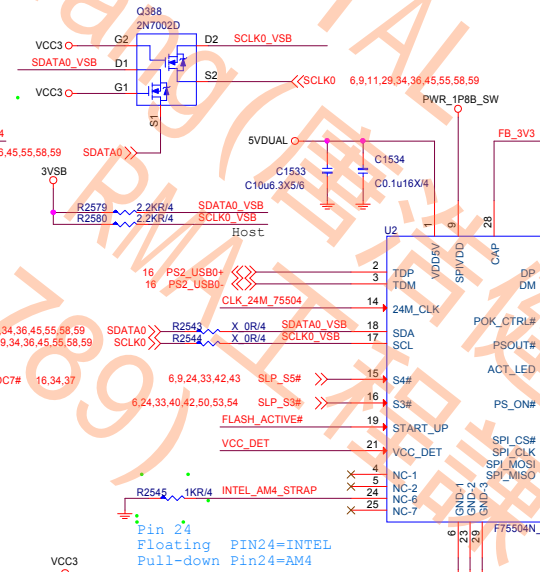
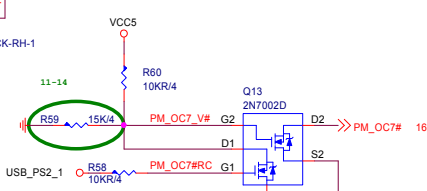
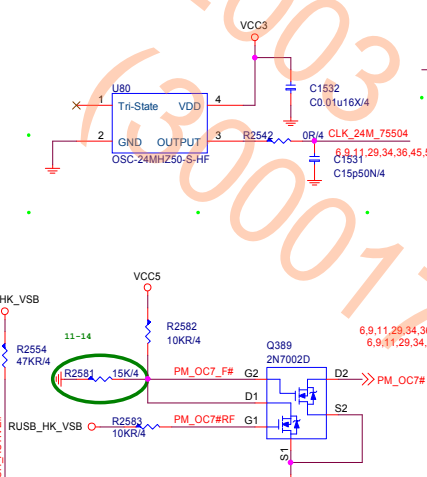
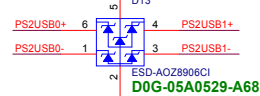
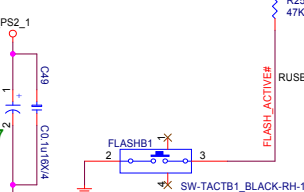


CLK running in S0, don't require in sleep



layout note:

- C21 must close to TVS pin5
- TVS must near KB\_MS1 connector and route without branch
- Varistor must close to TVS and route without branch




R fine tune by signal quality.

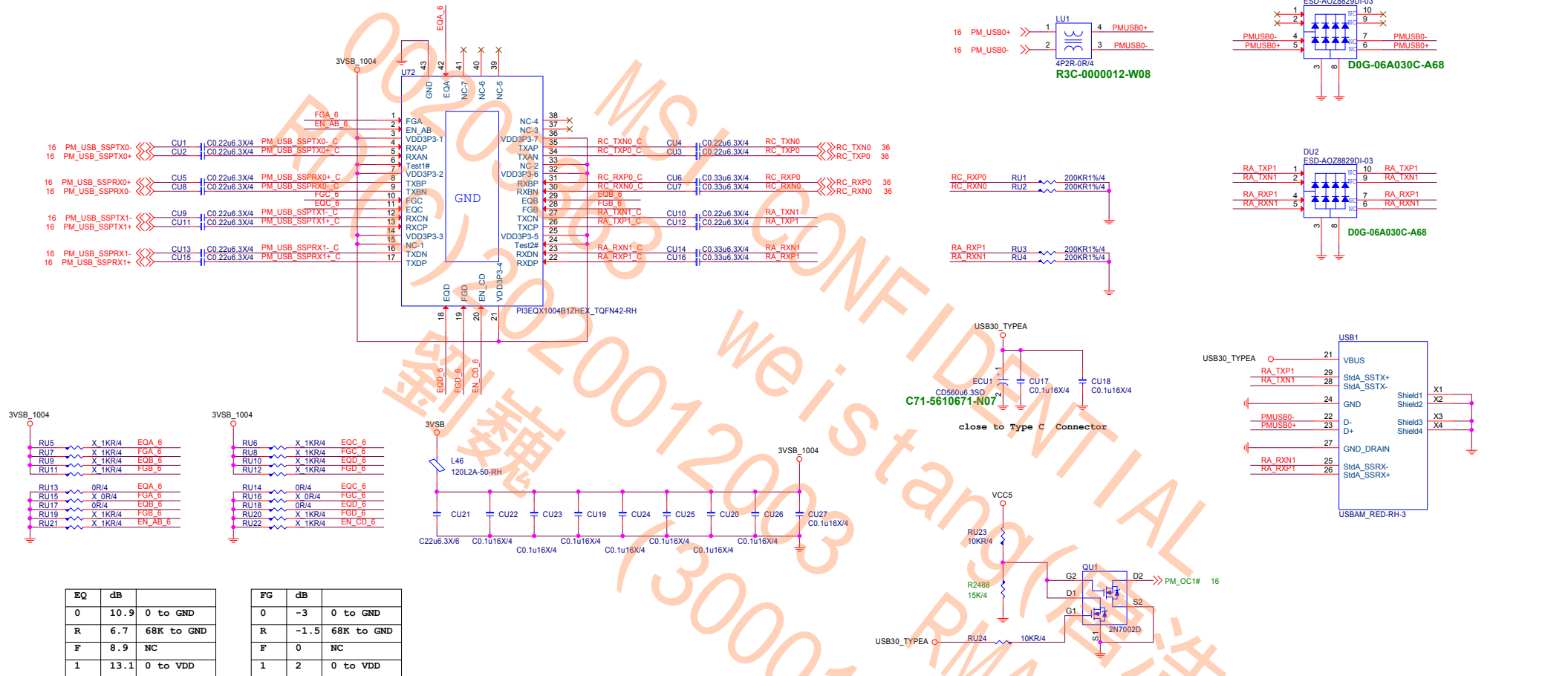
LED close to USB port

LED1

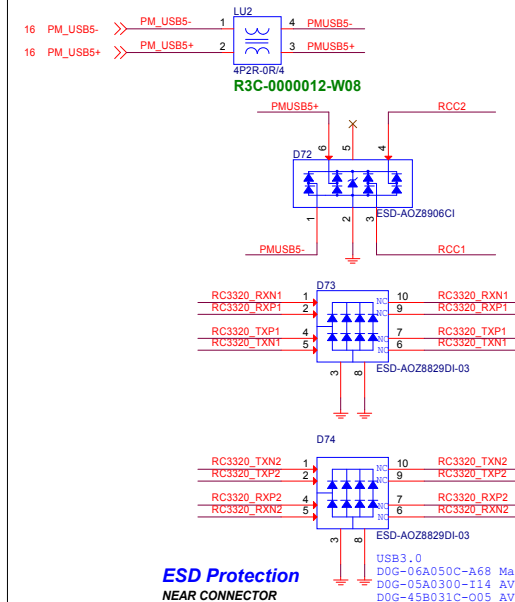
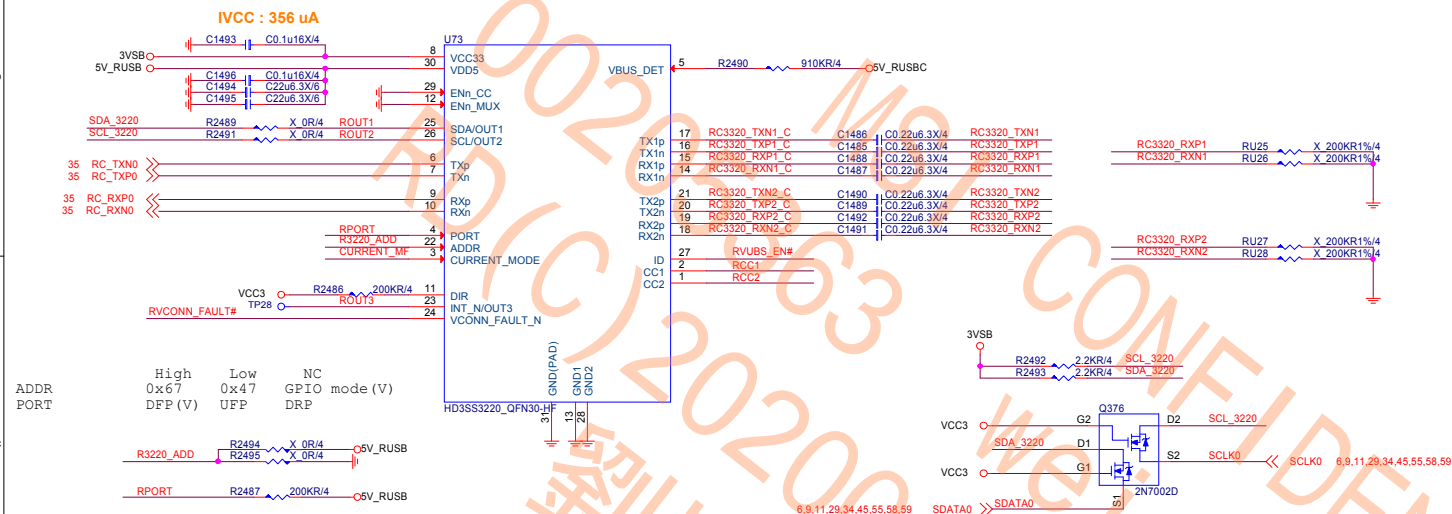
▶

 <b>MSI</b> <i>Always Be There For You</i>				<b>MICRO-START INT'L CO.,LTD.</b>			
<b>Title</b> <b>Rear PS2_USB2.0/LAN_USB3.0/FLASH SPI</b>							
<b>Size</b> Custom		<b>Document Number</b> <b>MS-7B85</b>				<b>Rev</b> <b>11</b>	
<b>Date:</b> Friday, June 29, 2018		<b>Sheet</b> 34		<b>of</b> 75			

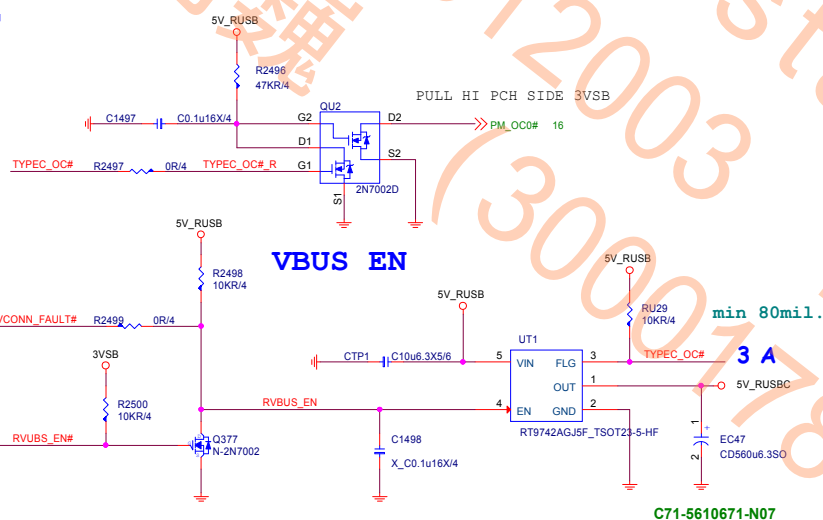
# TYPE-A PI3EQX1004 Redriver



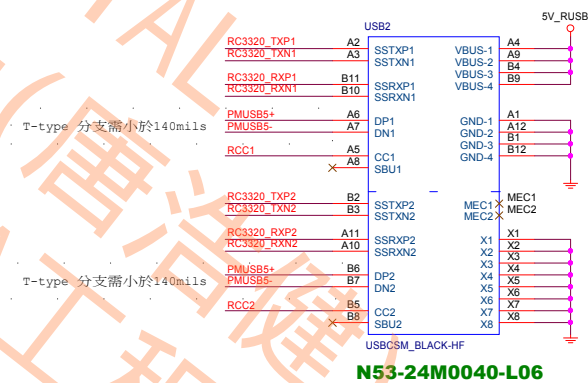
### USB 3.1-Type-C USB Type-C MUX with Configuration Channel (CC)



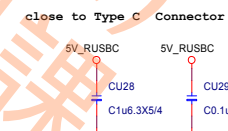
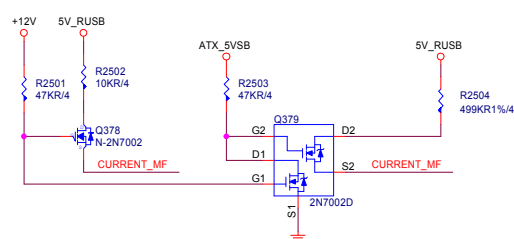
## VBUS OC# LEVEL SHIFT



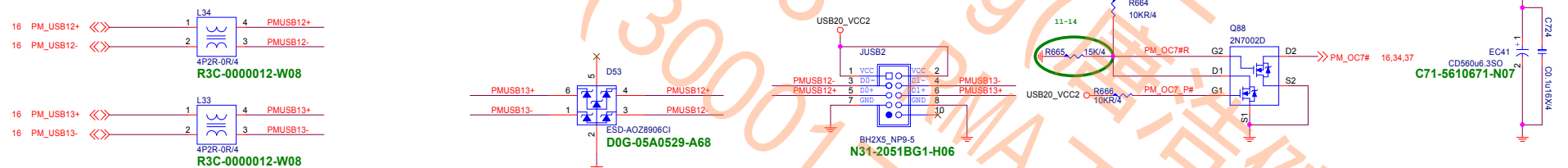
## VCOM OC#



## Current Mode



## 5V@1A



# Front USB3 180° BOX Header(JUSB4)

5V@1.8A

16 PM\_USB\_SSTX0+ <<< C695 C0.22u6.3X/4 PM\_SSTX0+  
16 PM\_USB\_SSTX0- <<< C694 C0.22u6.3X/4 PM\_SSTX0-

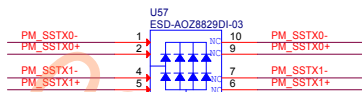
16 PM\_USB\_SSRX0+ <<< C693 C0.33u6.3X/4 PMUSB\_SSRX0+  
16 PM\_USB\_SSRX0- <<< C692 C0.33u6.3X/4 PMUSB\_SSRX0-

16 PM\_USB10+ <<< L35 4 PMUSB10+  
16 PM\_USB10- <<< 2 3 PMUSB10-  
4P2R-0R/4  
R3C-0000012-W08

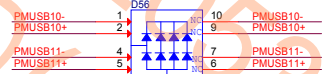
16 PM\_USB11+ <<< L36 4 PMUSB11+  
16 PM\_USB11- <<< 2 3 PMUSB11-  
4P2R-0R/4  
R3C-0000012-W08

16 PM\_USB\_SSTX1+ <<< C689 C0.22u6.3X/4 PM\_SSTX1+  
16 PM\_USB\_SSTX1- <<< C688 C0.22u6.3X/4 PM\_SSTX1-

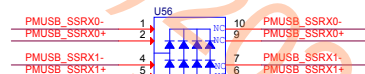
16 PM\_USB\_SSRX1+ <<< C687 C0.33u6.3X/4 PMUSB\_SSRX1+  
16 PM\_USB\_SSRX1- <<< C686 C0.33u6.3X/4 PMUSB\_SSRX1-



D0G-06A030C-A68

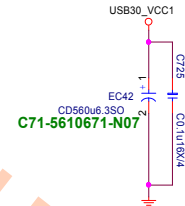
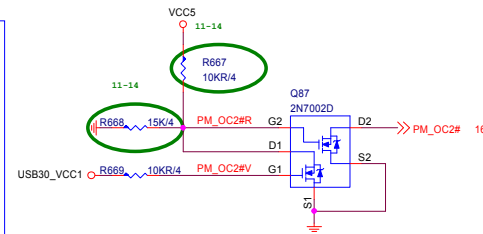
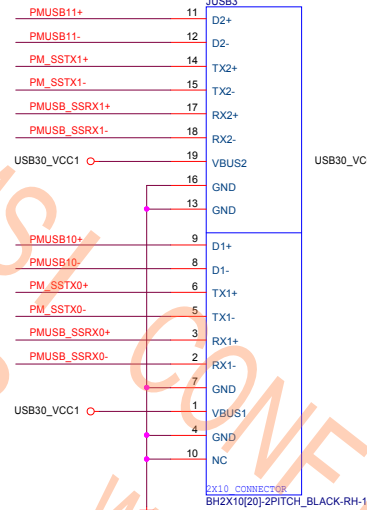


D0G-06A030C-A68



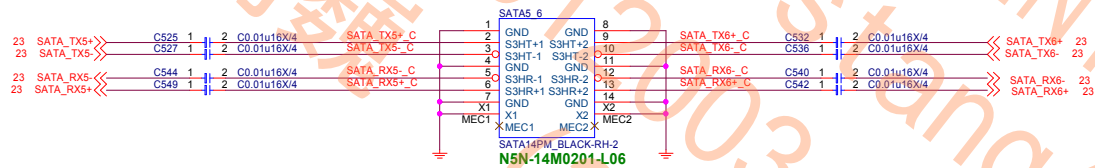
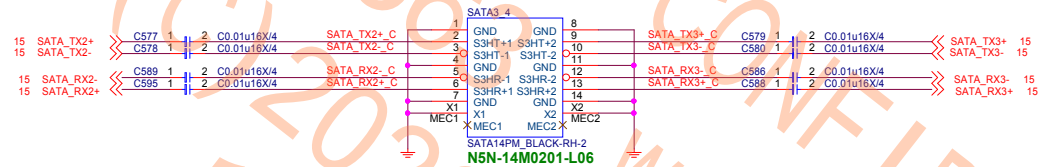
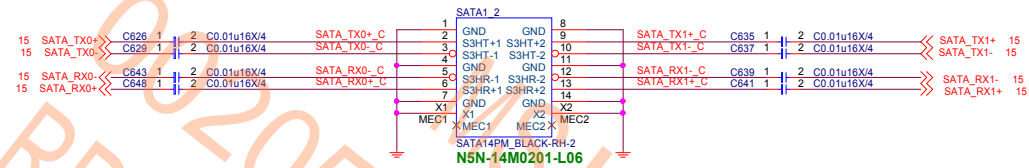
D0G-06A030C-A68

USB3.0  
D0G-06A050C-A68 Main  
D0G-05A0300-I14 AVL  
USB2.0  
D0G-0200529-A68 Main  
D0G-0100619-I05 AVL






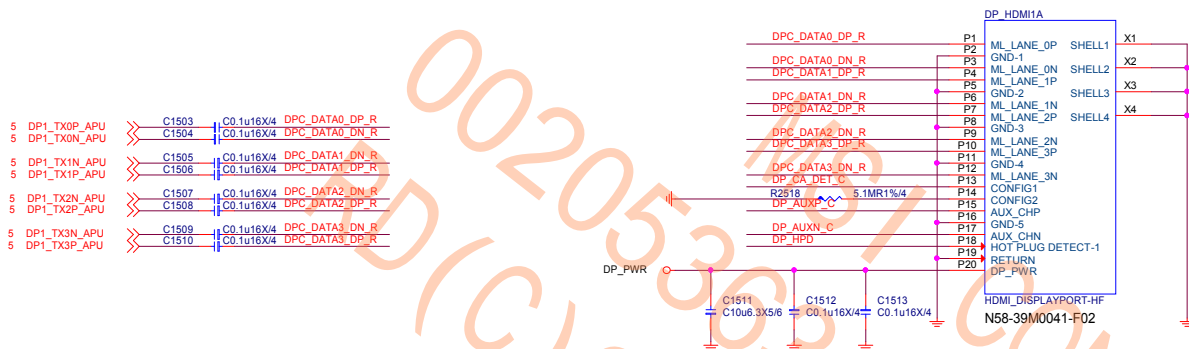
## SATA Connector



Schematic Cfg	Project	
CFG-7B85-10-Performance Gaming	V	A
CFG-7B85-20-Arsenal Gaming		

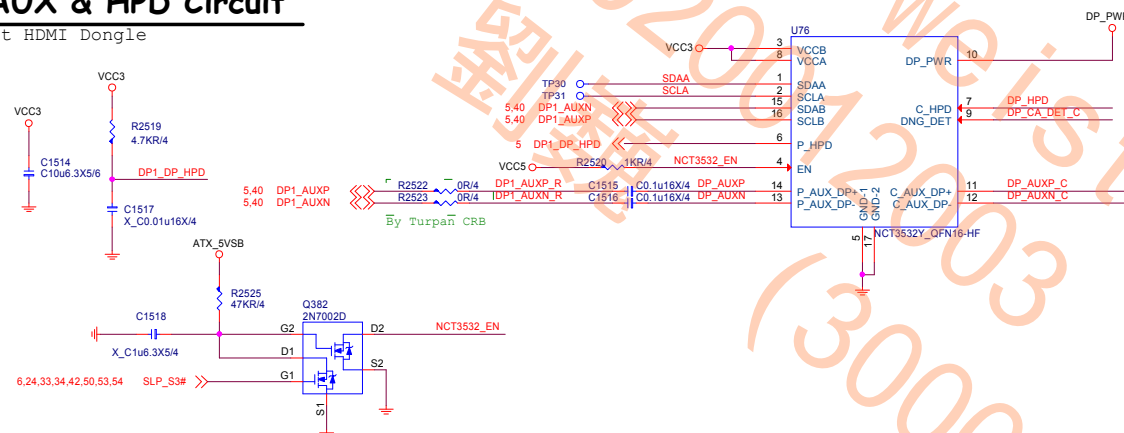
 <b>MICRO-START INT'L CO.,LTD.</b>		
File <b>SATA</b>		
Size	Document Number	Rev
Custom	<b>MS-7B85</b>	<b>11</b>
Date: Friday, June 29, 2018	Sheet 39 of 75	

## DP CONNECTOR

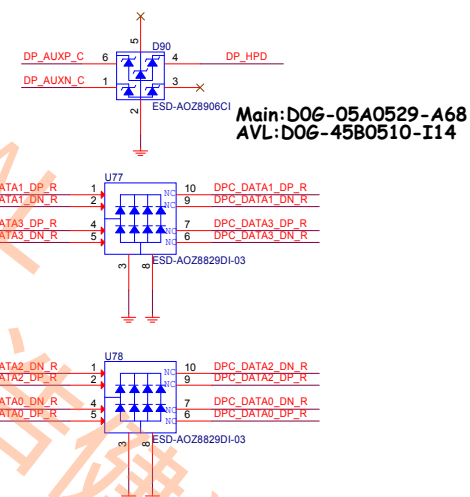


## DP AUX & HPD Circuit

Support HDMI Dongle

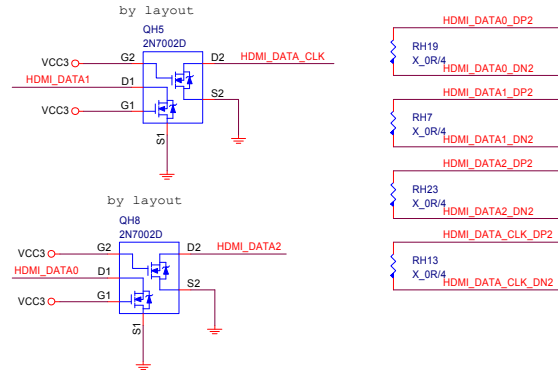
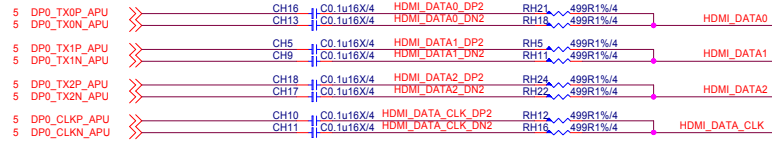


## ESD

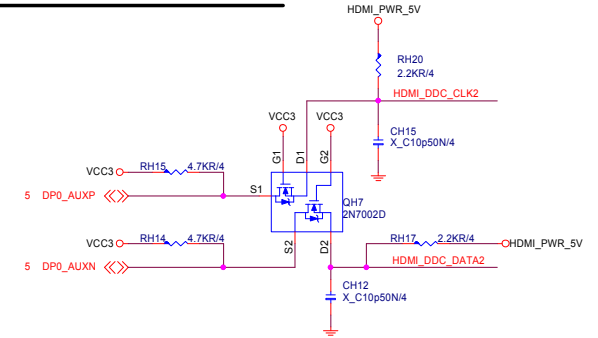


# HDMI CONNECTOR

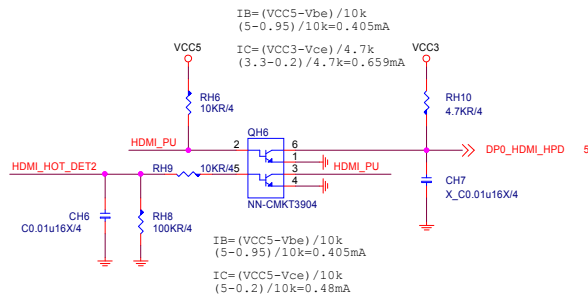
For HDMI 1.4



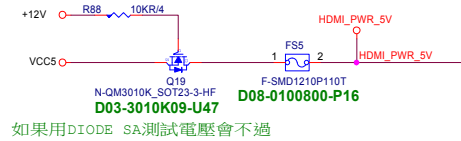
# AUX Level Shifter



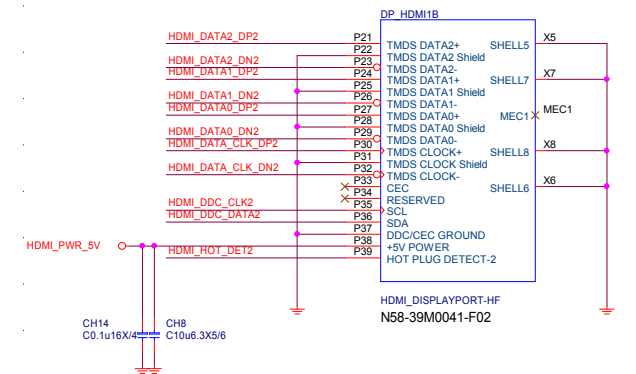
# HPD Circuit



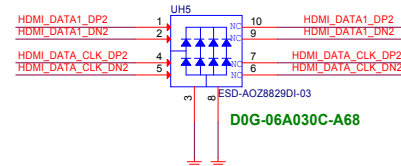
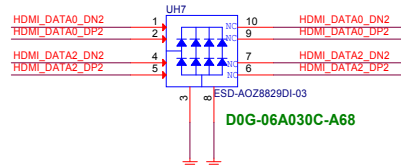
# Connector Power



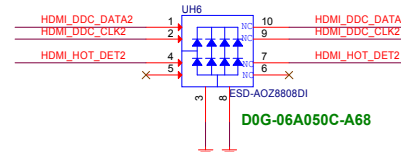
# Connector



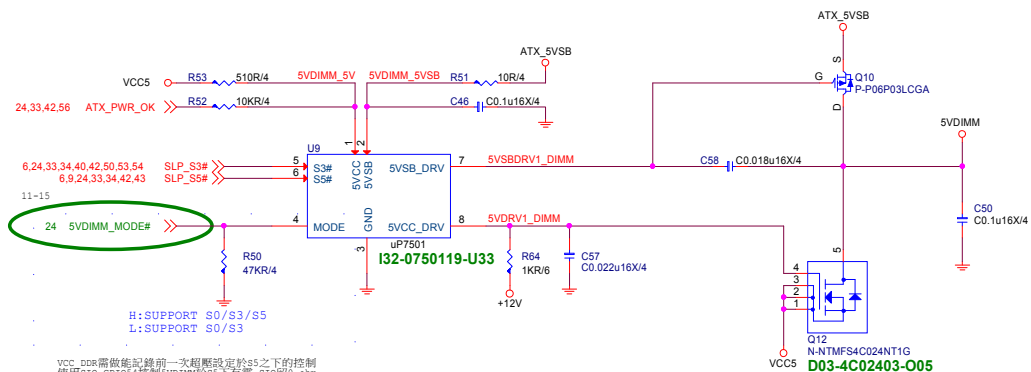
# For EMI



注意:耐壓5v零件



## 5VDIMM FOR DDR



## 3VSB cost down

3.3V@2.63A

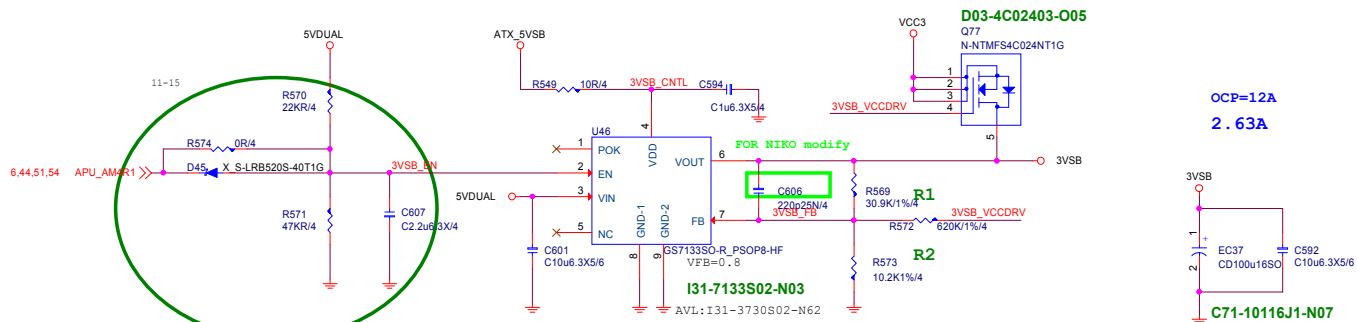
1.05V@0.05A

VDDBT\_RTC G@4.5uA

***FCH@0.07A***

CPU@0.25A

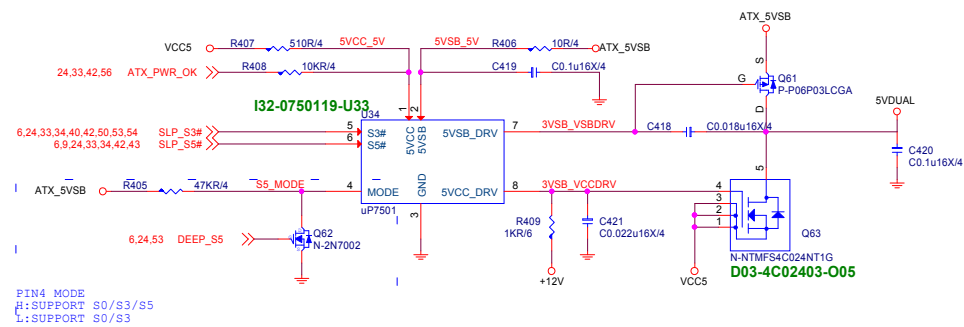
PCIE\*6 @2.25A



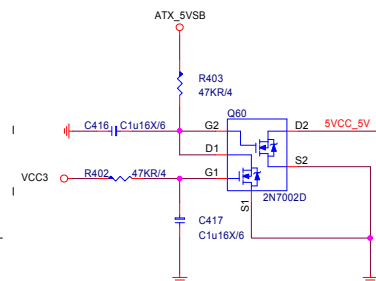
VFB=3.224V for S0->S3 3VSB voltage raise & ATX\_5VSB drop.

$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (30.9K/10.2K)) \\ &= 3.22V \end{aligned}$$

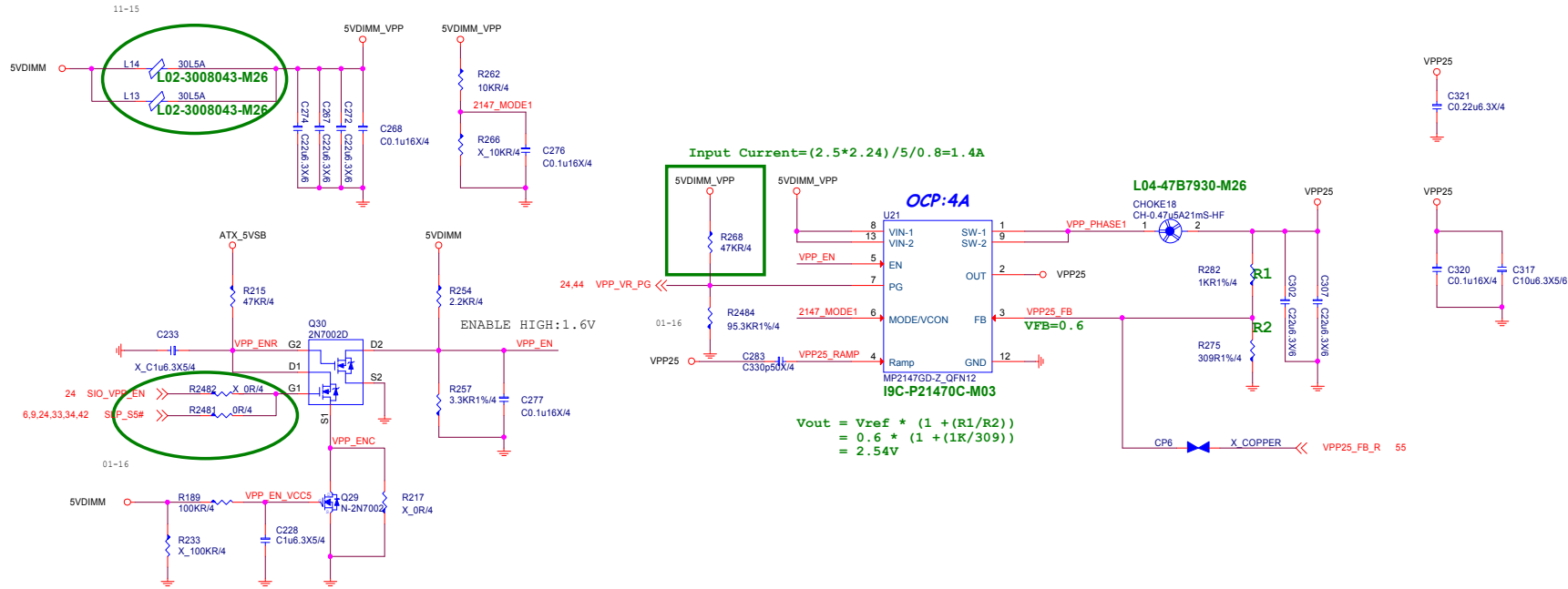
## 5VDUAL For 3VSB、CPU 1.8V、VDDP



For power 700W solution (only for uP7501+uP7506 for 3VSB solution)  
The power supply VCC3 delay 12ms after VCC5 assert.  
The chip U7501 5VDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but  
VCC3 not ready and let the 3VSB sequence fail.

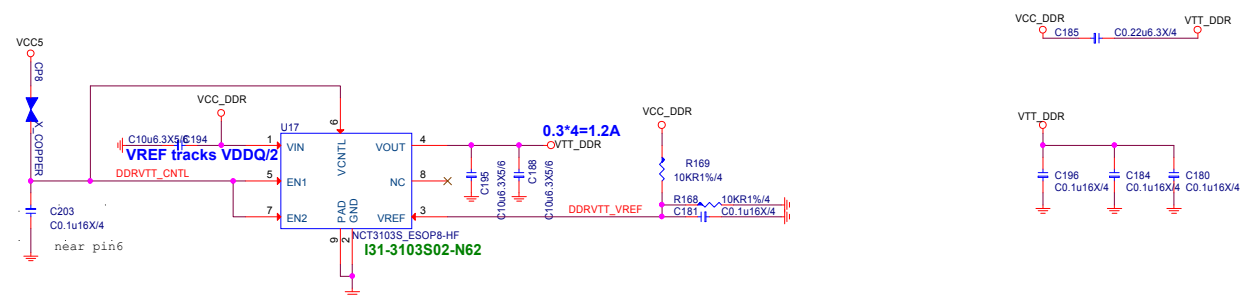


**4DIMM : VPP25**  
**2.5V@2.24A**



### DDR VTT Power

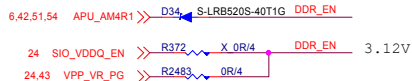
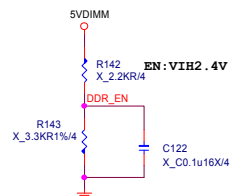
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



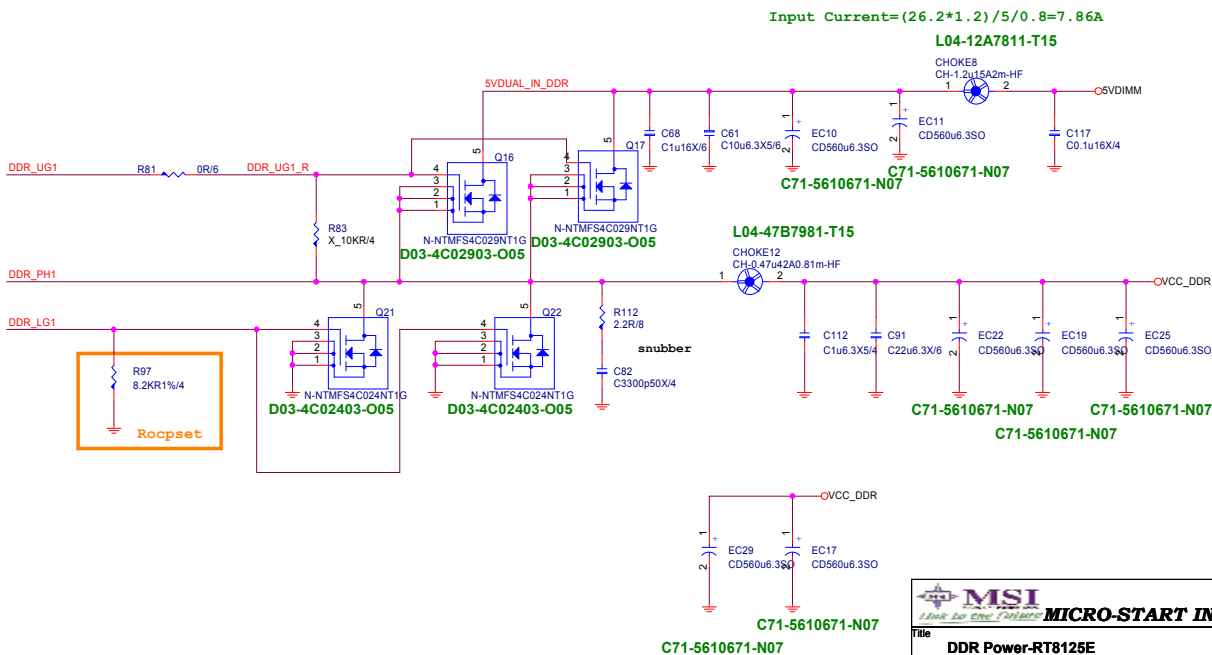
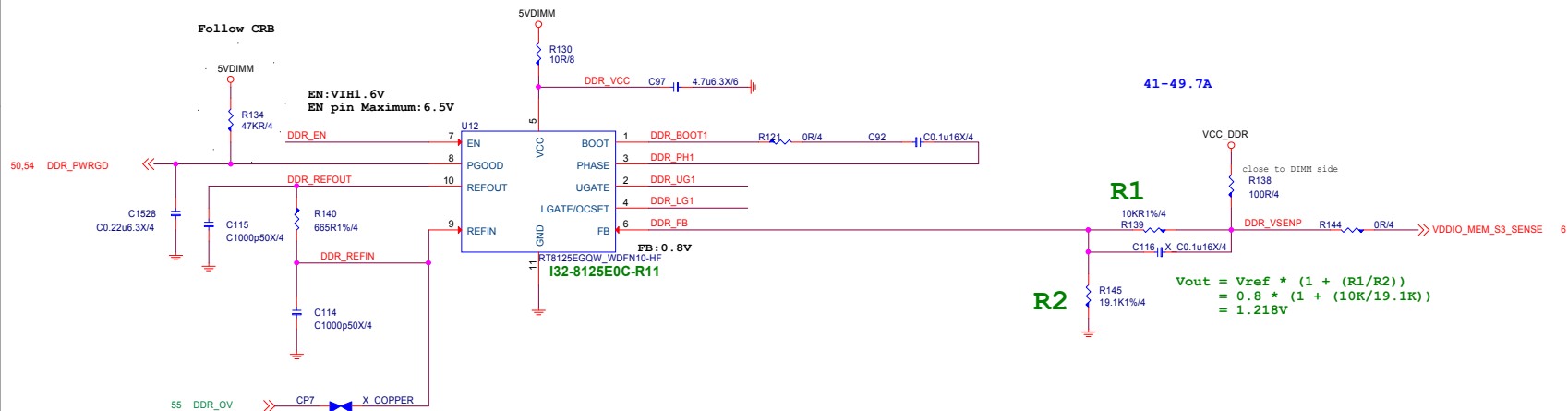
# DDR4\_1.2V@26.2A

15.5A FOR CPU  
9.5A FOR 4DIMM  
1.2A FOR DDR VTT

Rocpset: 6.8K  
OCP=Rocset\*10uA/Rdson(Low side)  
=6.8K\*10uA/2mohm  
=34A

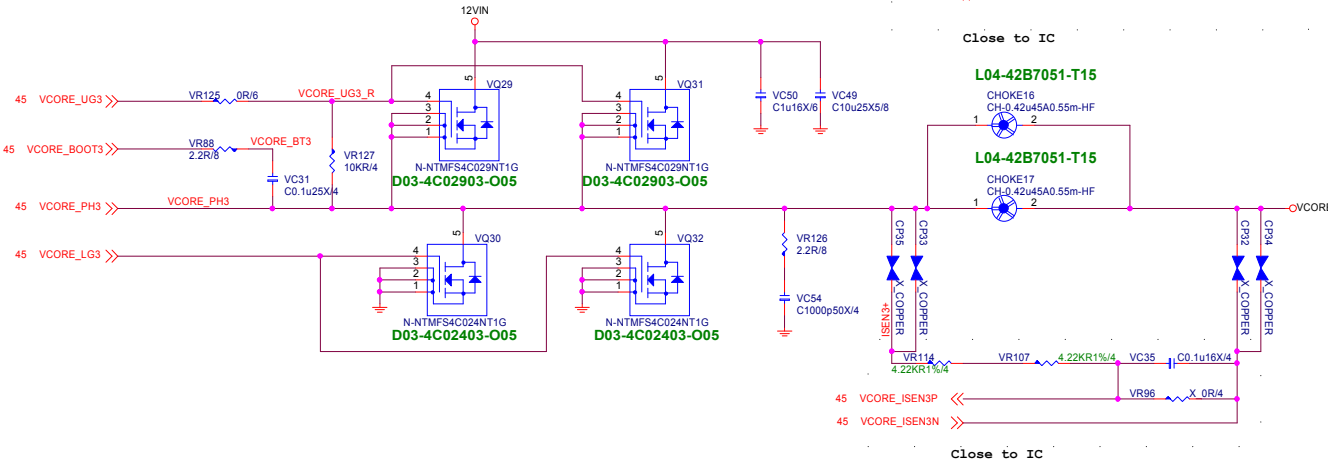


EN: VIH2.4V  
EN pin Maximum: 5.5V, RECOMMENDED: 3.6V



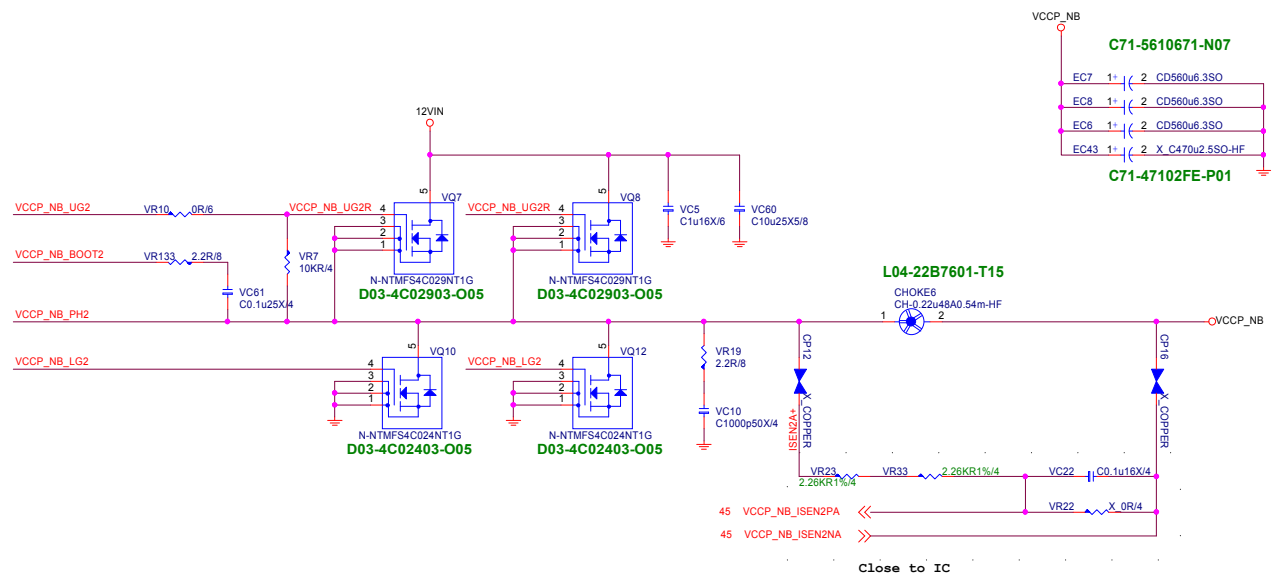
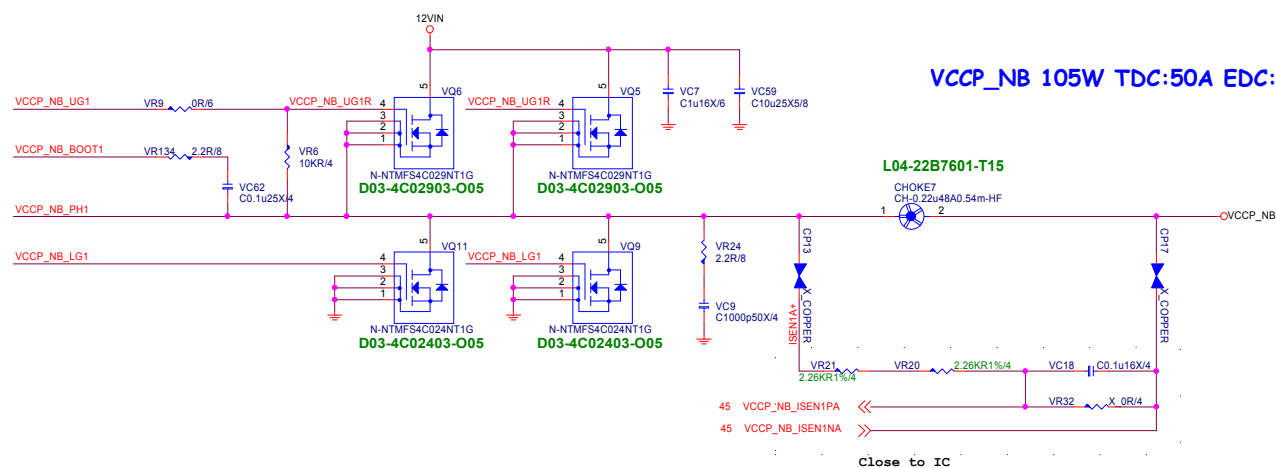
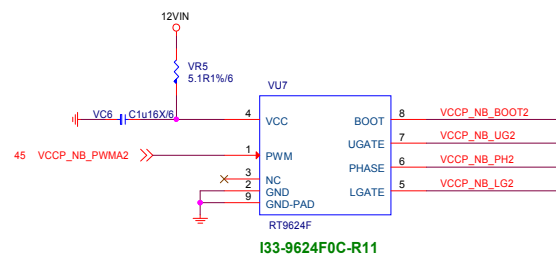
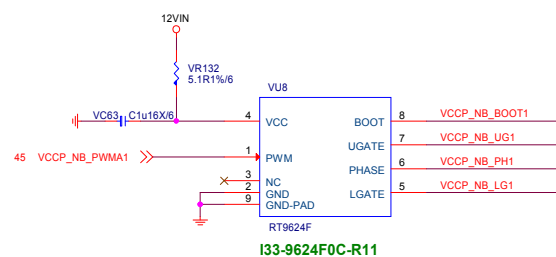








VCCP\_NB 105W TDC:50A EDC:75A

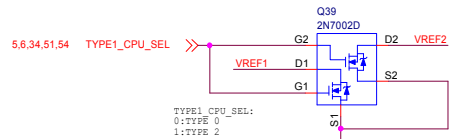
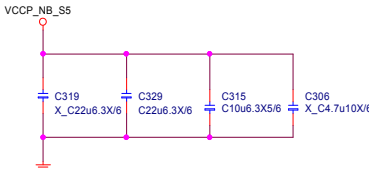
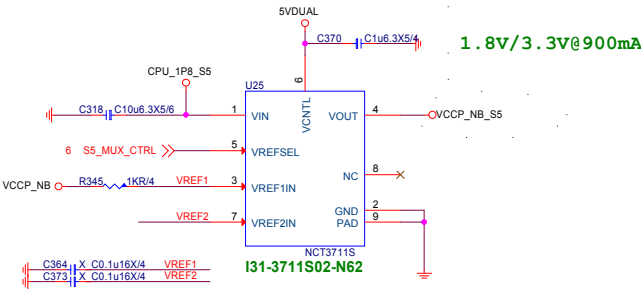
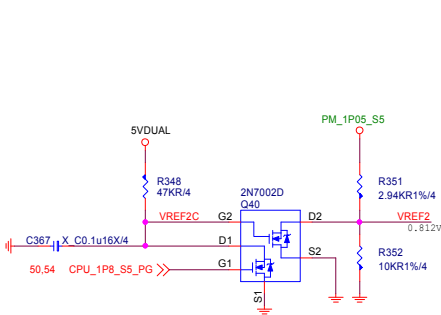


FOR  
VCCP\_SOC\_S5  
0.9A

S5\_MUX\_CTRL  
HIGH:S0  
LOW: S3/S5

H: +VDDCR\_FCH\_ALW will track VDDNB  
L: If VDDCR\_SOC<0.775V (OR 0.85V),VDDCR\_SOC\_S5 =0.775V.  
If VDDCR\_SOC >= 0.775V (OR 0.85V) , VDDCR\_SOC\_S5 will track VDDCR\_NB

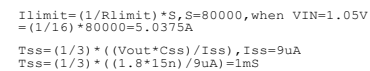
(VDDCR\_SOC\_S5 is only used for AMD Family 15h Models 60h-6Fh processors)



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	2	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP\_NB\_S5 ONLY SUPPORT TYPE0

```
1.8V S5@0.5A
1.8V S0@2A
0.9A(VCCP_NB_S5)
```





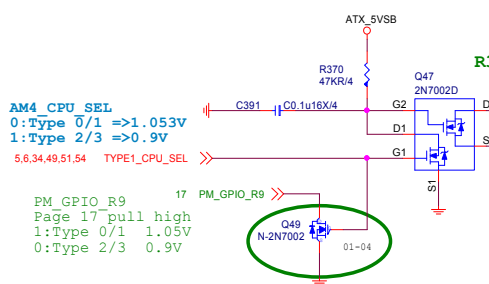
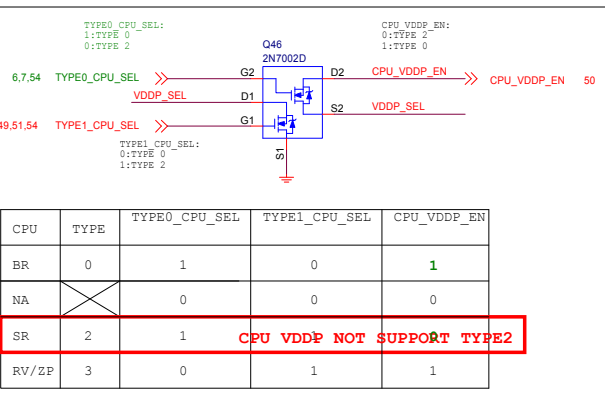
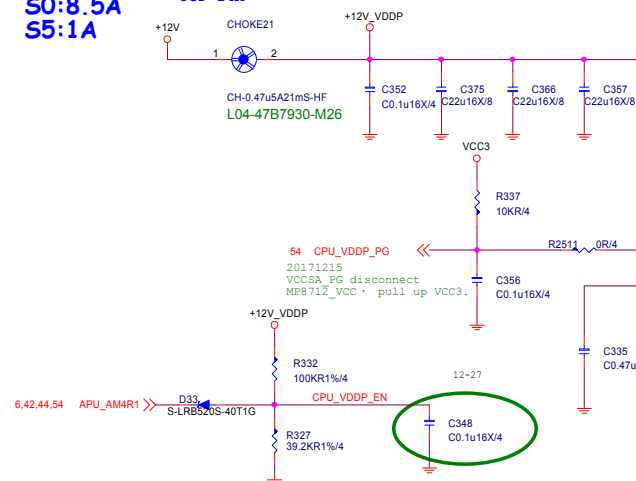
## CPU\_VDDP\_S0

1.05V/0.9V@S0:8.5A

S0:8.5A  
S5:1A

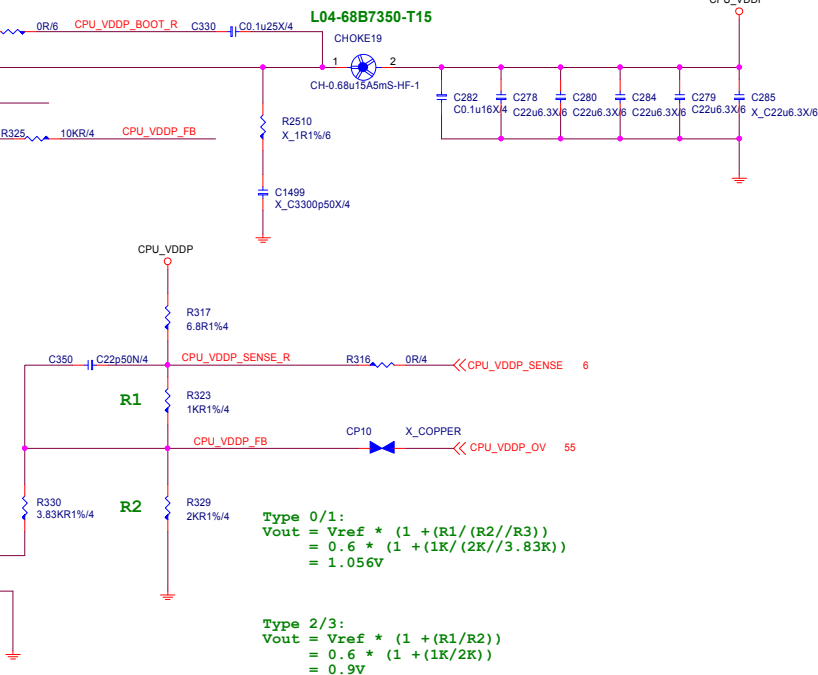
OCP=14A

Input Current= (8.5A\*1.05V)/12V/0.8=0.93A



OCP=14A

1.05V, 8.5A



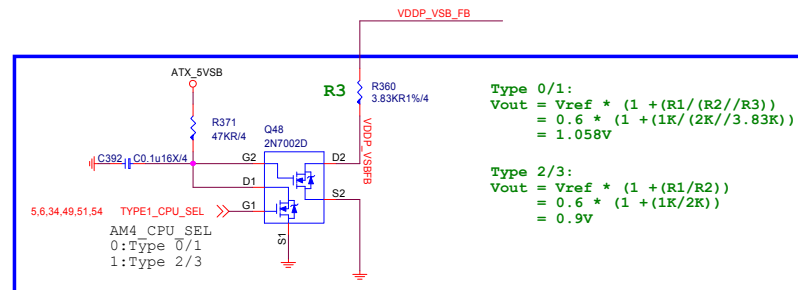
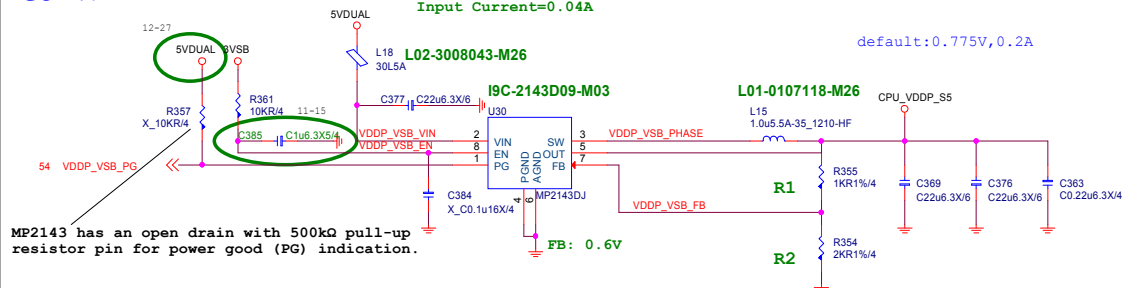
## CPU\_VDDP\_S5

1.05V/0.9V  
S5:1A

(VDDCR\_SOC\_S5 is only used for AMD TYPE0)

Input Current=0.04A

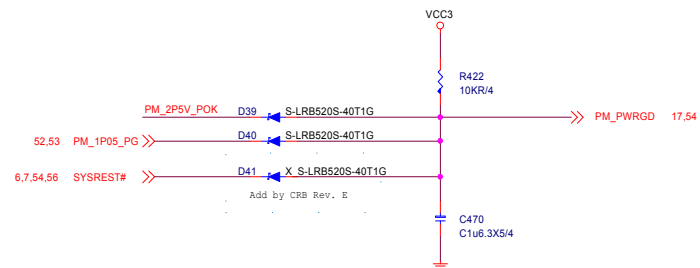
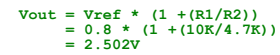
default:0.775V,0.2A



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File  
CPU Power VDDP  
Size  
Custom  
Document Number  
MS-7B85  
Date  
Friday, June 29, 2018  
Sheet  
51  
of  
75  
Rev  
11

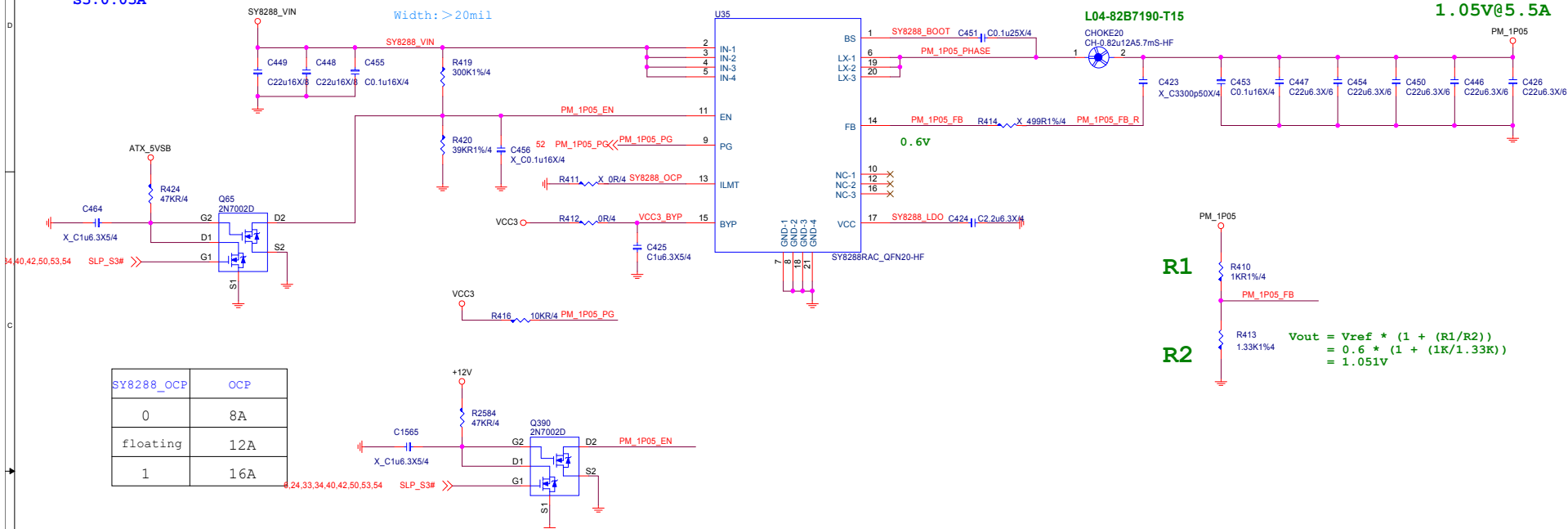
## 2.5V@900mA



## FOR Promontory 1.05V\_S0

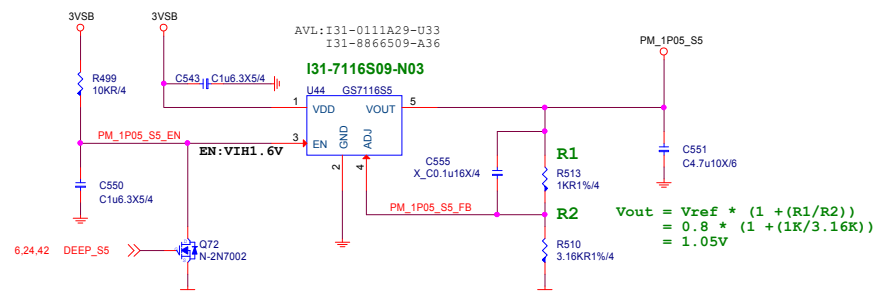
1.05V  
S0:5.5A  
S5:0.05A

+12V CHOKE22 SY8288\_VIN  
L04-47B7930-M26  
CH-0.47u5A21mS-HF  
Input Current= (5.5A\*1.05V)/12V/0.8=0.6A

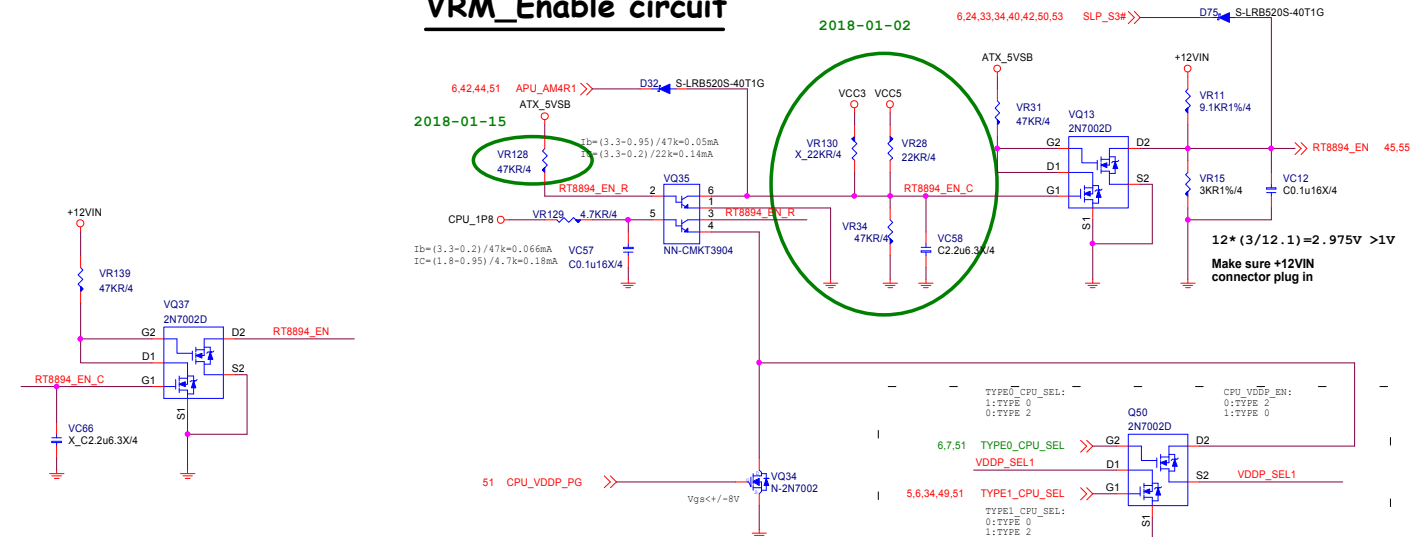



## FOR Promontory 1.05V\_S5

1.05V@0.05A

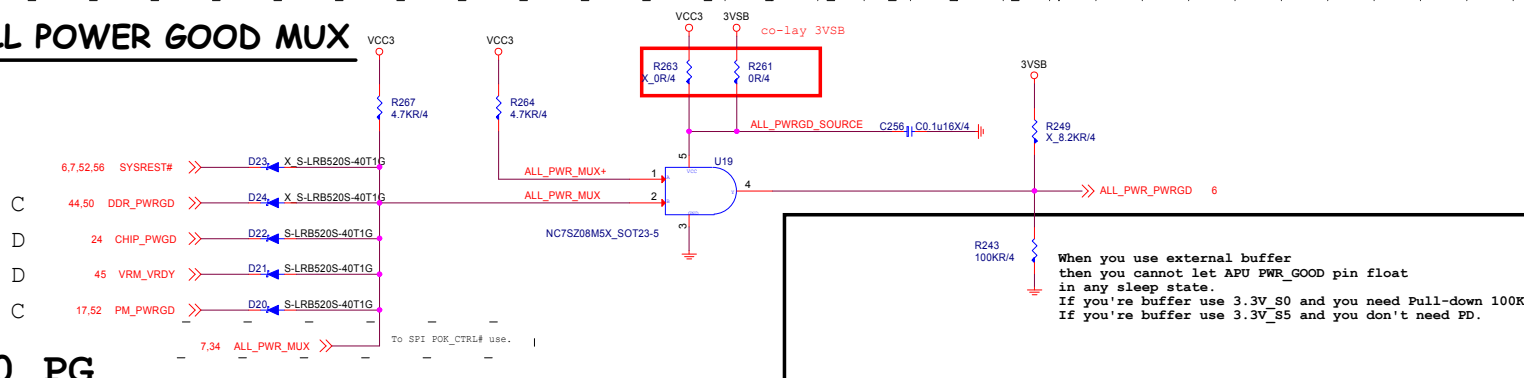


## VRM\_Enable circuit

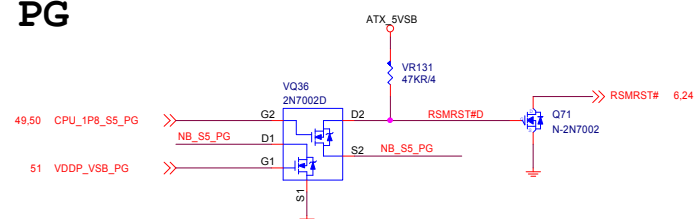


CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/3P	3	1	0

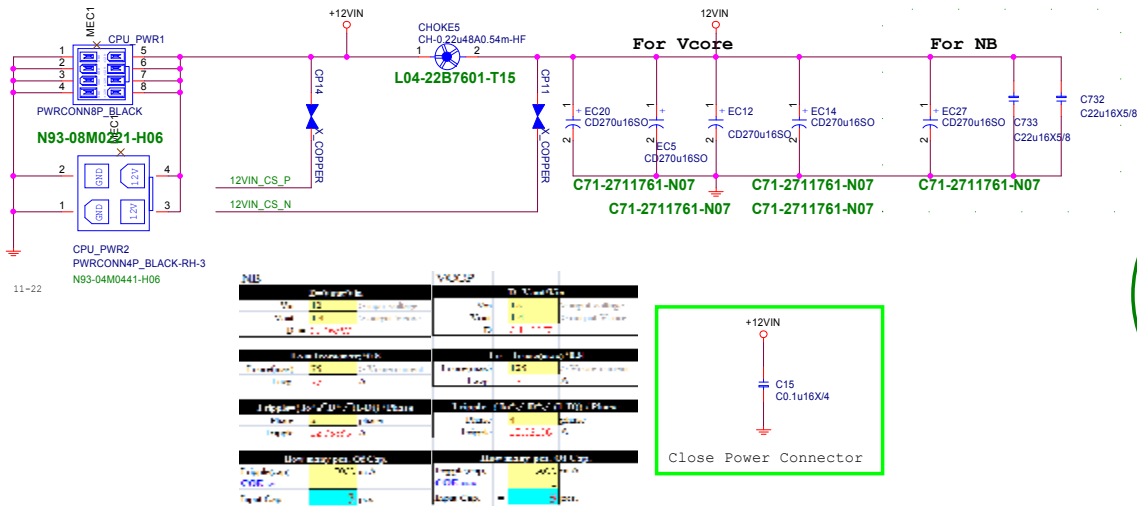
ALL POWER GOOD MUX



S0	PG
<hr/>	
S5	PG

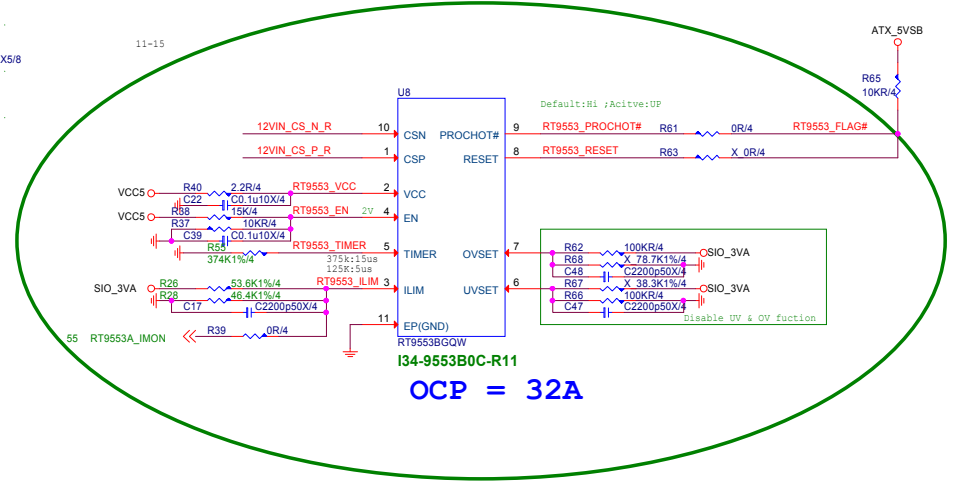


## CPU POWER CONNECTOR



## RT9553B CURRENT SENSE

RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.

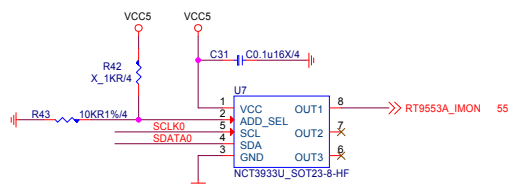


## Over Voltage Control IC

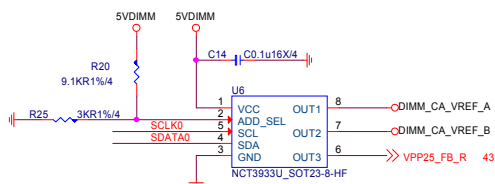
### UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

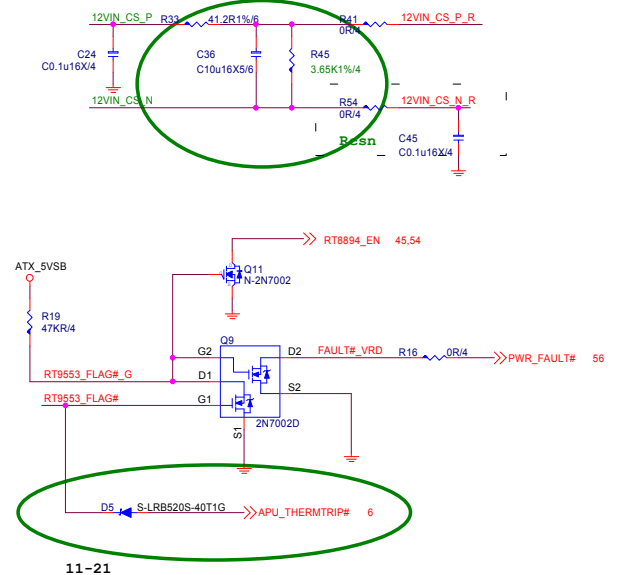
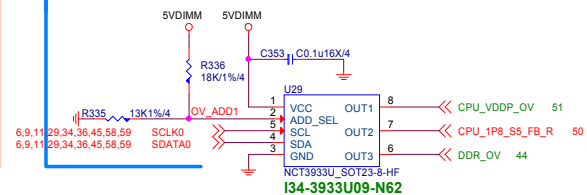
0x2A: RH=OPEN, RL=10K



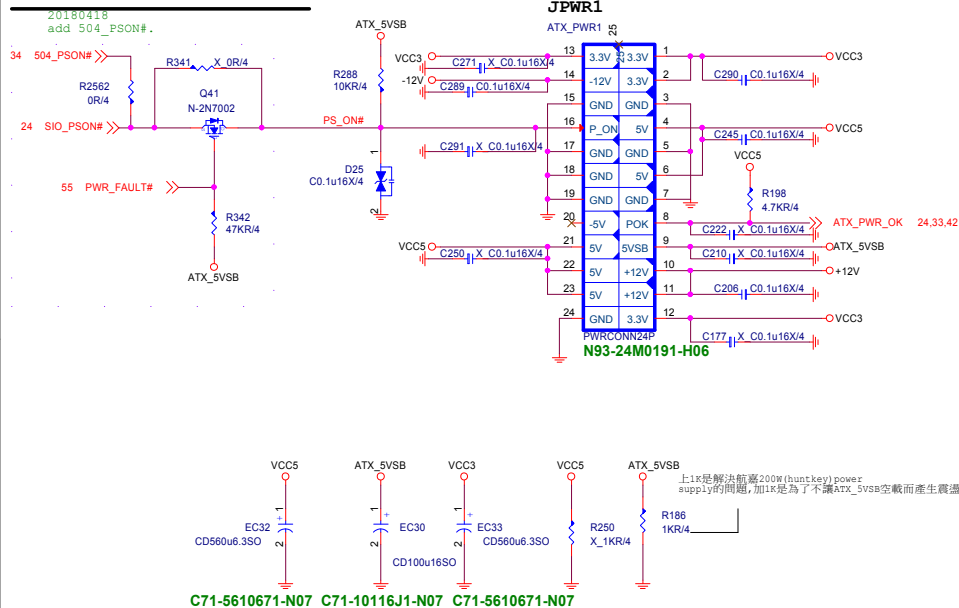
0x28: RH=9.1K, RL=3K



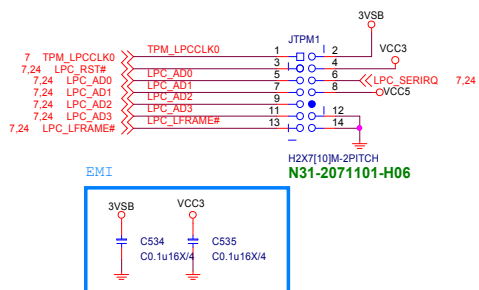
0x26: RH=18K, RL=13K



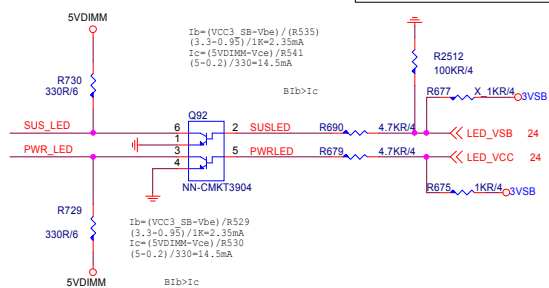
## ATX POWER CONNECTOR



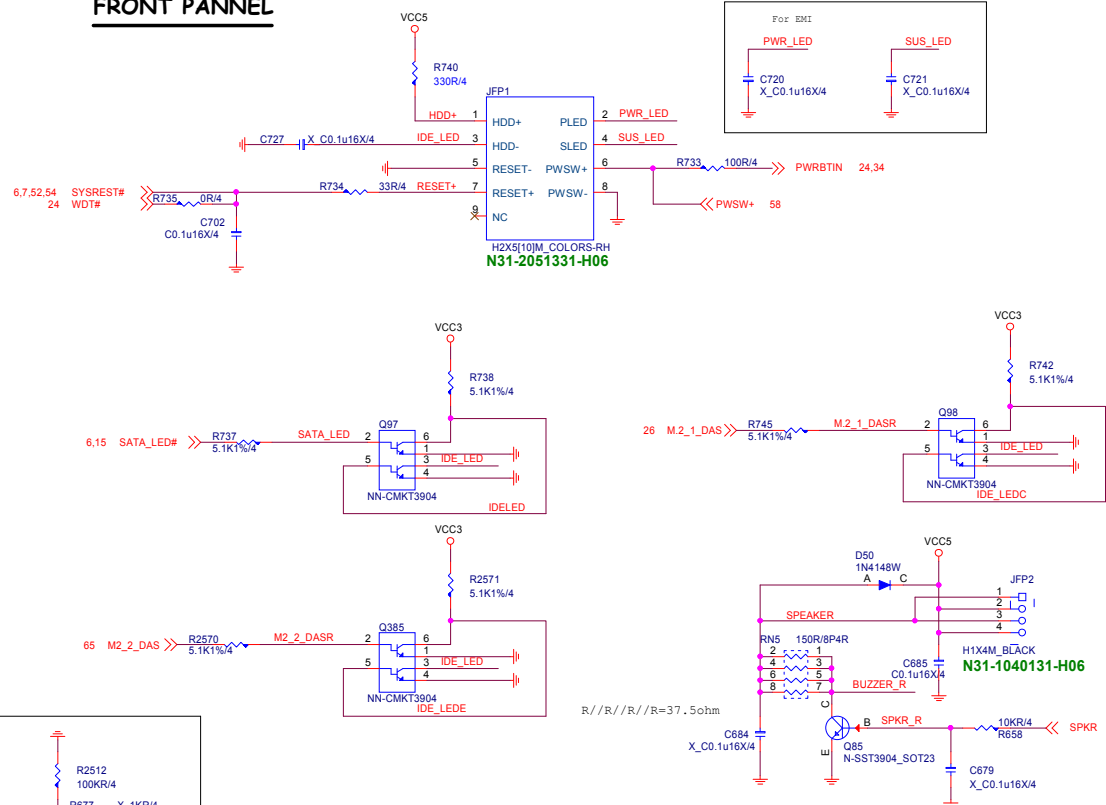
## TPM



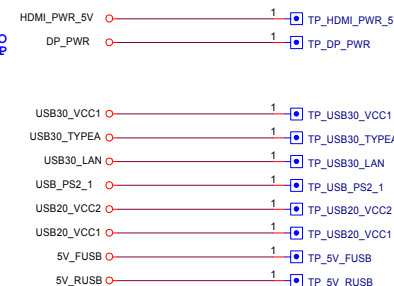
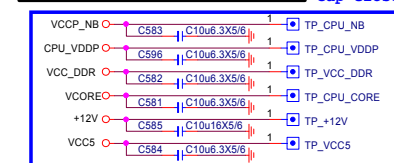
## LED ( for NCT6797)



## FRONT PANNEL



## Voltage Mearsure Point



**MSI**  
MICRO-START INT'L CO.,LTD.

File: **ATX/Front Panel**

Size: Custom  
Document Number: **MS-7B85**

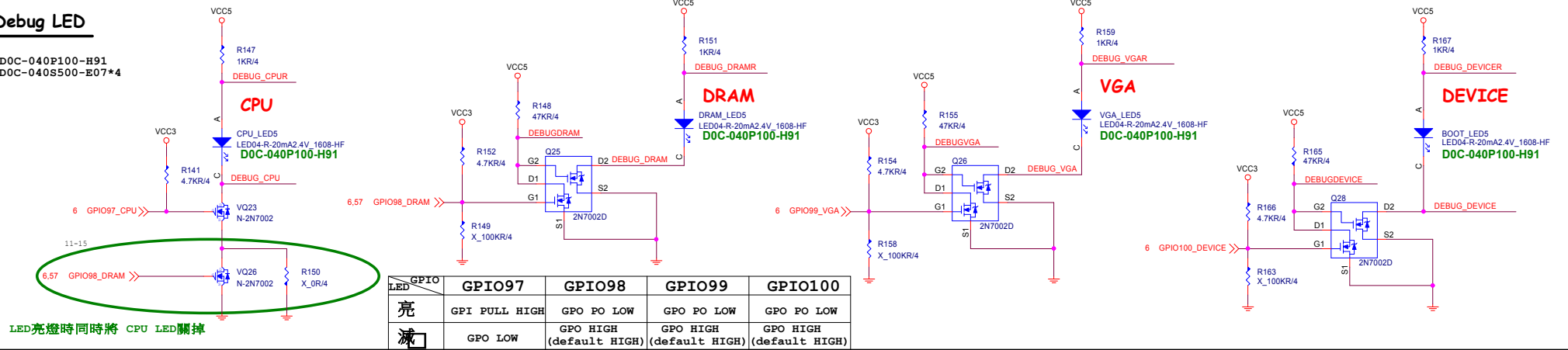
Date: Friday, June 29, 2018  
Sheet: 56 of 75

Rev: **11**

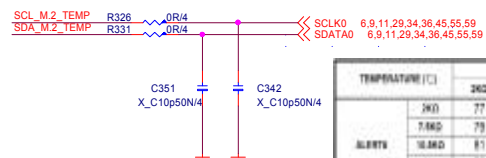
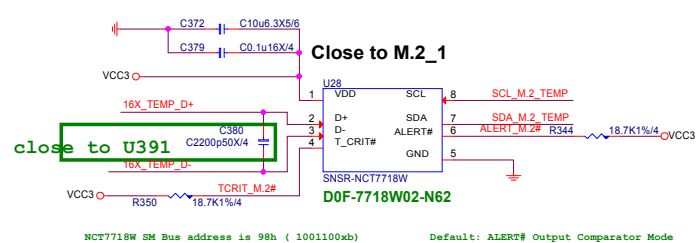


## EZ Debug LED

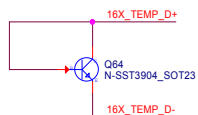
紅:M:D0C-040P100-H91  
S:D0C-040S500-E07\*4



# NCT7718W



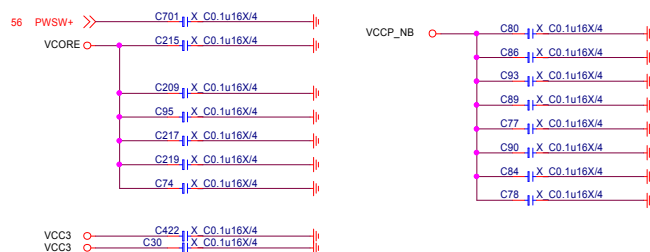
TEMPERATURE (°C)	T_CRIT					
	2K0	77	87	97	107	117
ALERT#	7.0K0	79	89	99	109	119
	10.0K0	81	91	101	111	121
	13.0K0	83	93	103	113	123
	16.7K0	85	95	105	115	125



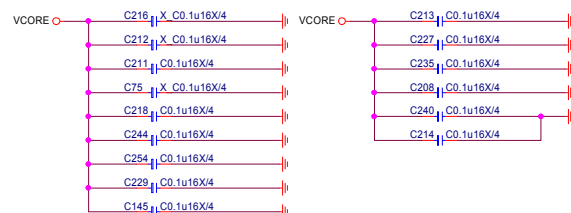
Layout notice:  
1. Put the C1 2200pF to close the NCT7718W.  
2. Add Ground Shielding For D+ and D- Traces.  
3. D+/D- Route Has to be Away From the High Noise Area.  
4. The Recommended Traces Width and Ground Shielding Spacing are 10mils.

Place to PCIe16X SLOT

Add for EMI

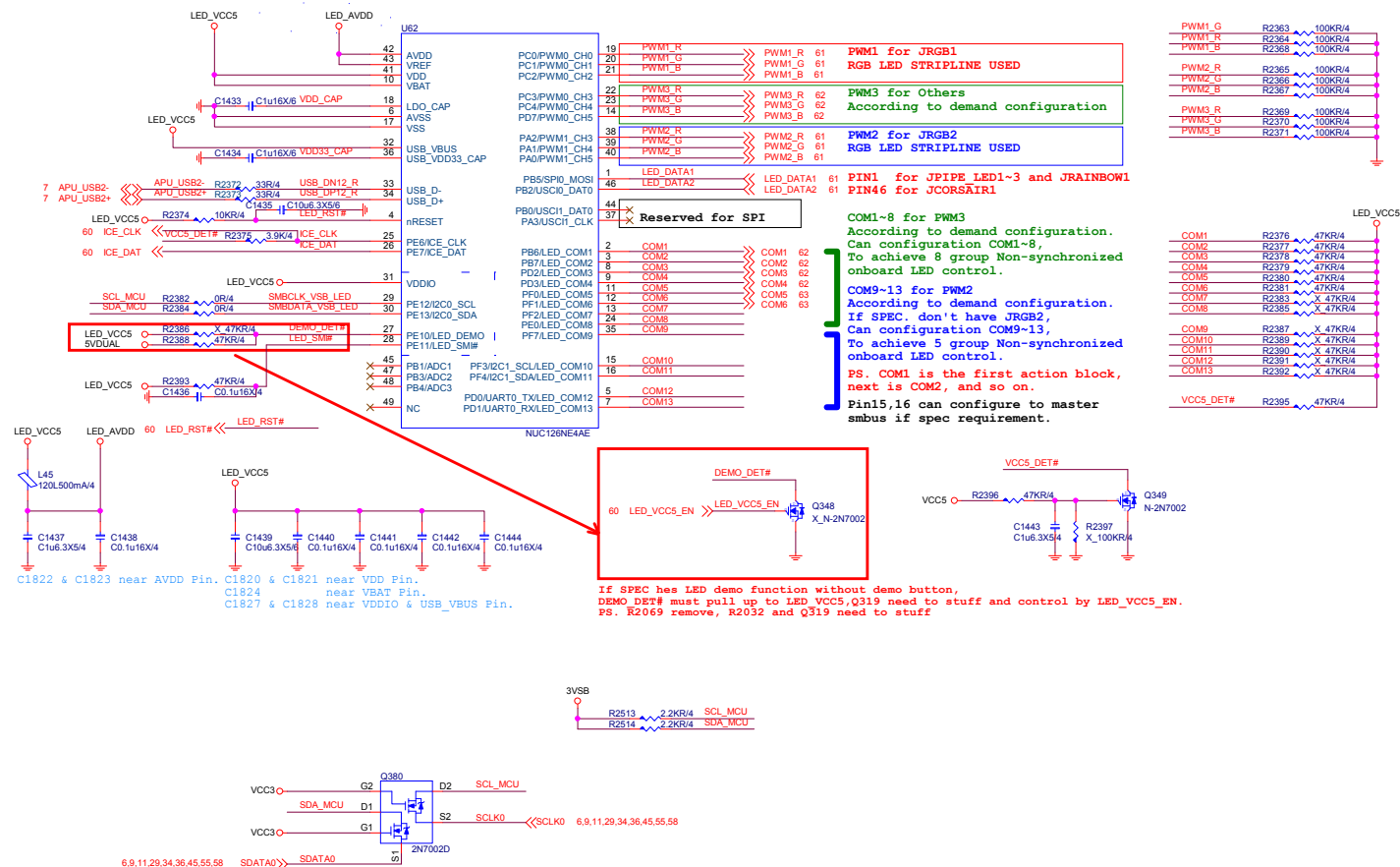


return path

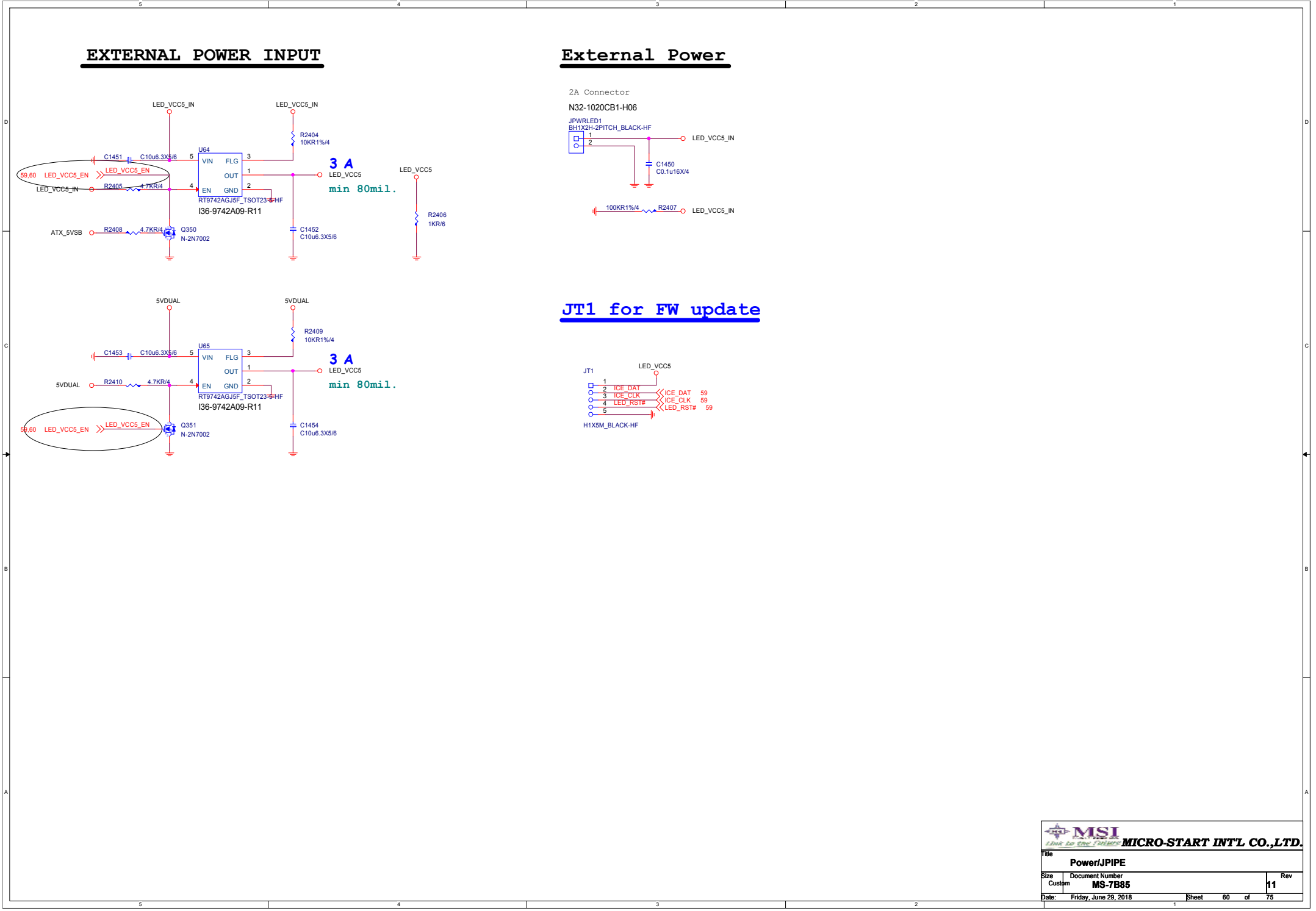
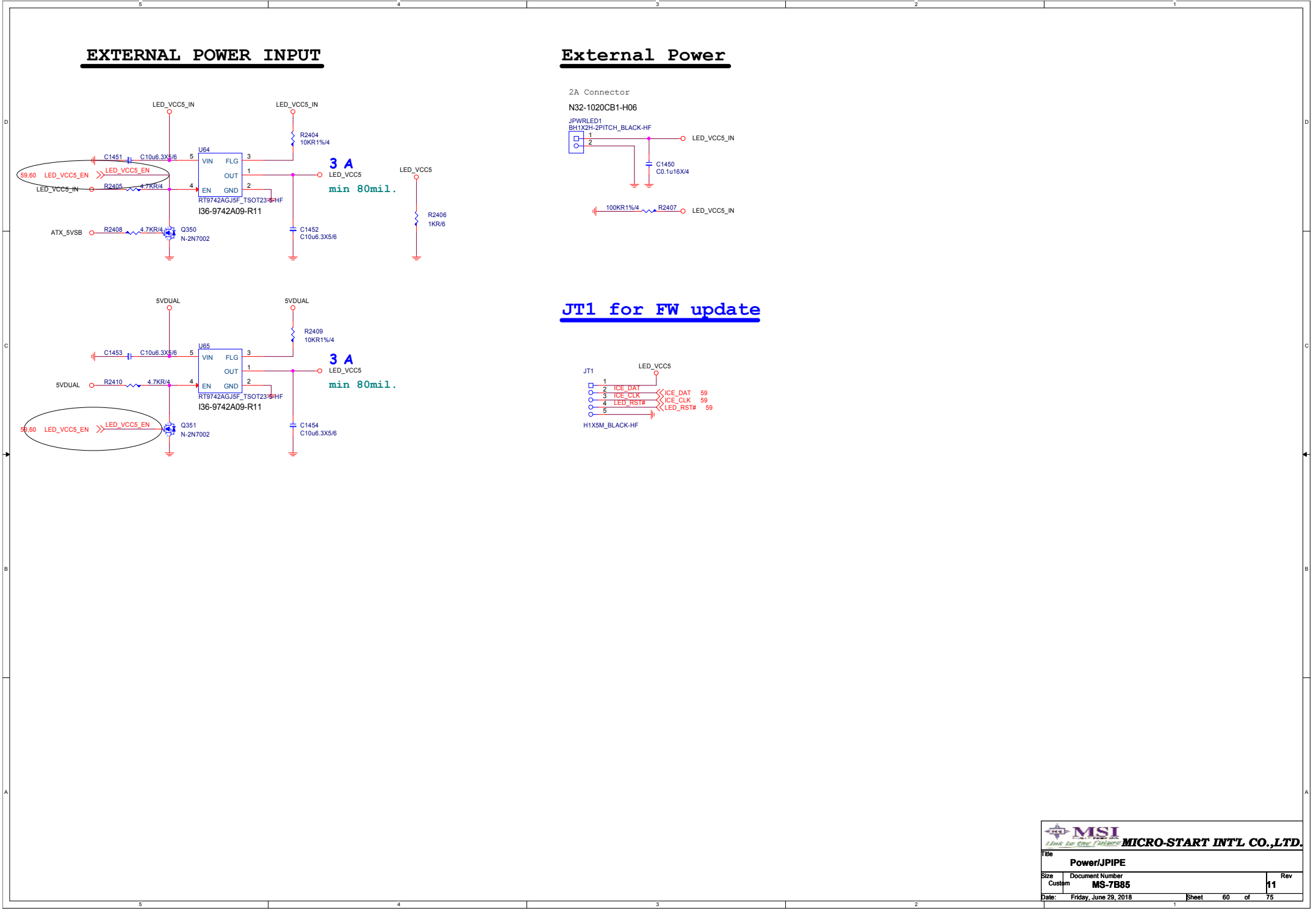
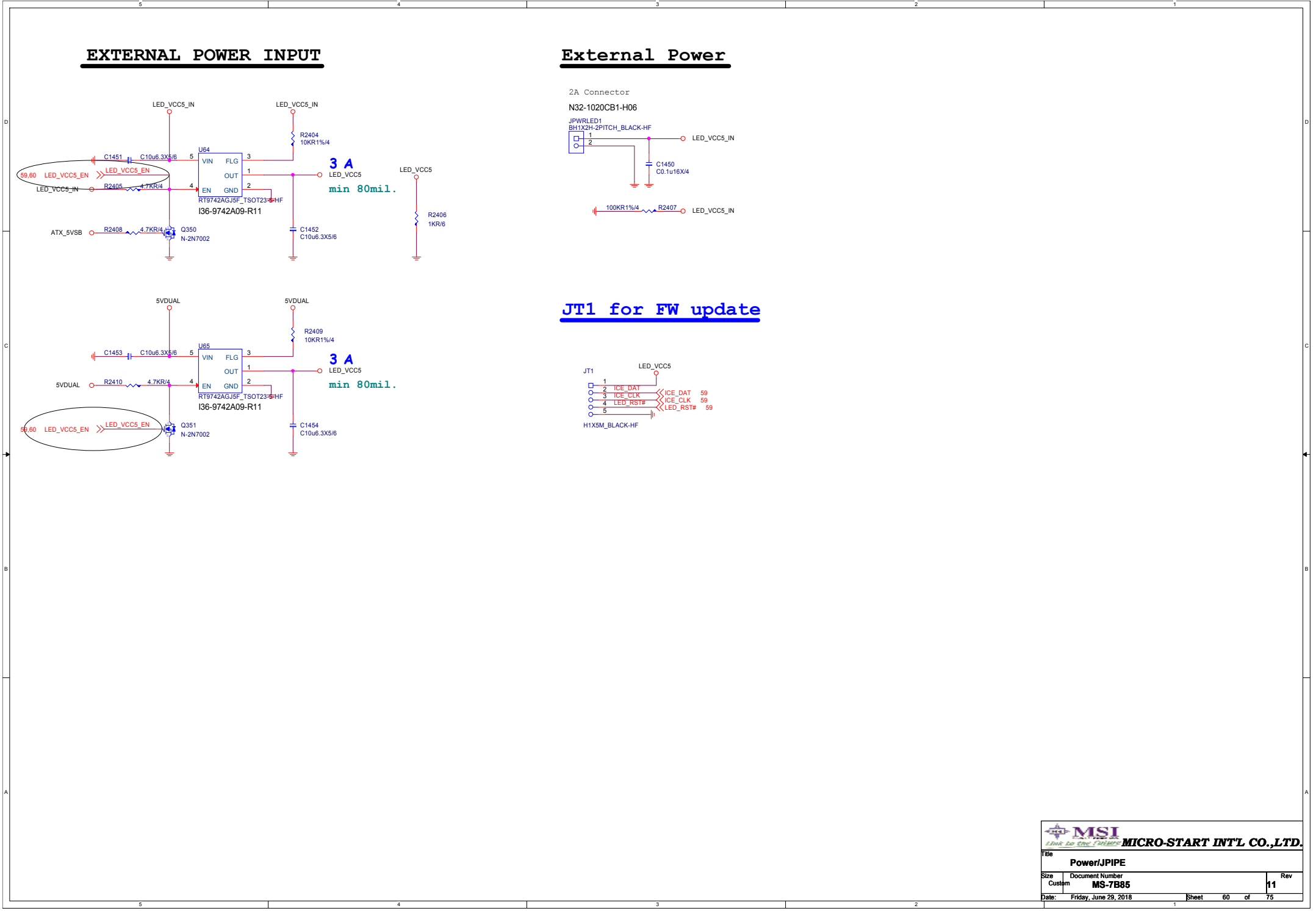


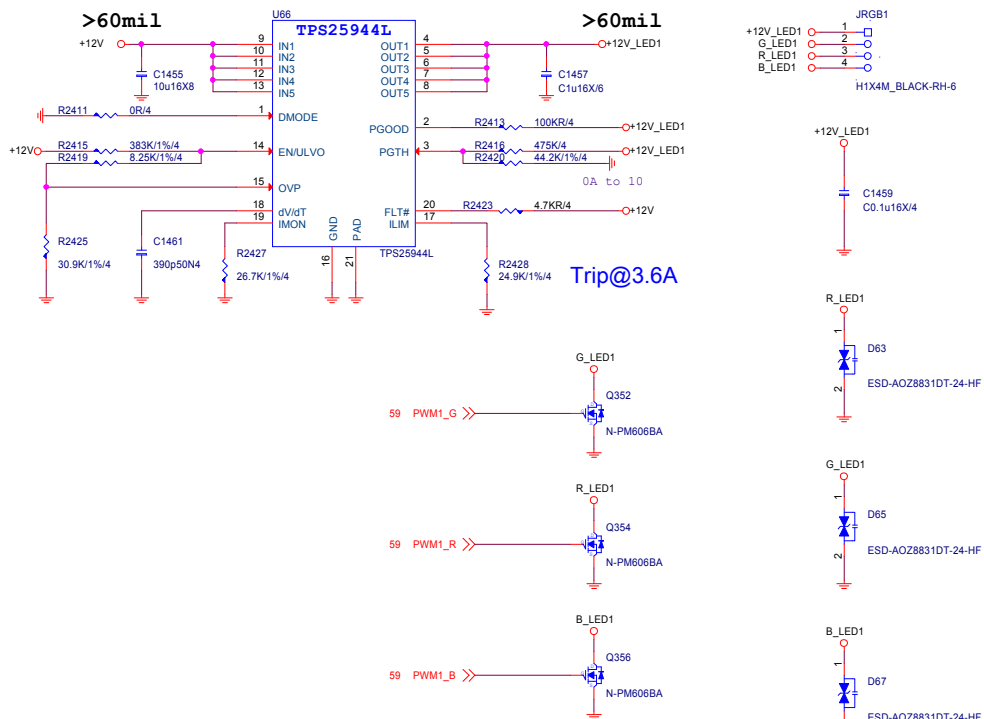
## 48 PIN LED MCU

If you use ADC function, need to separate VREF from AVDD and 4 09VREF stuff for VREF.

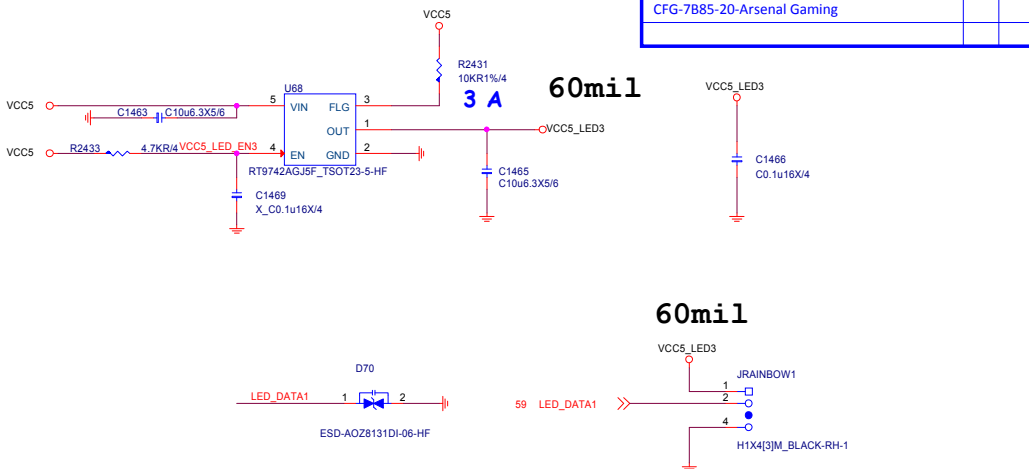
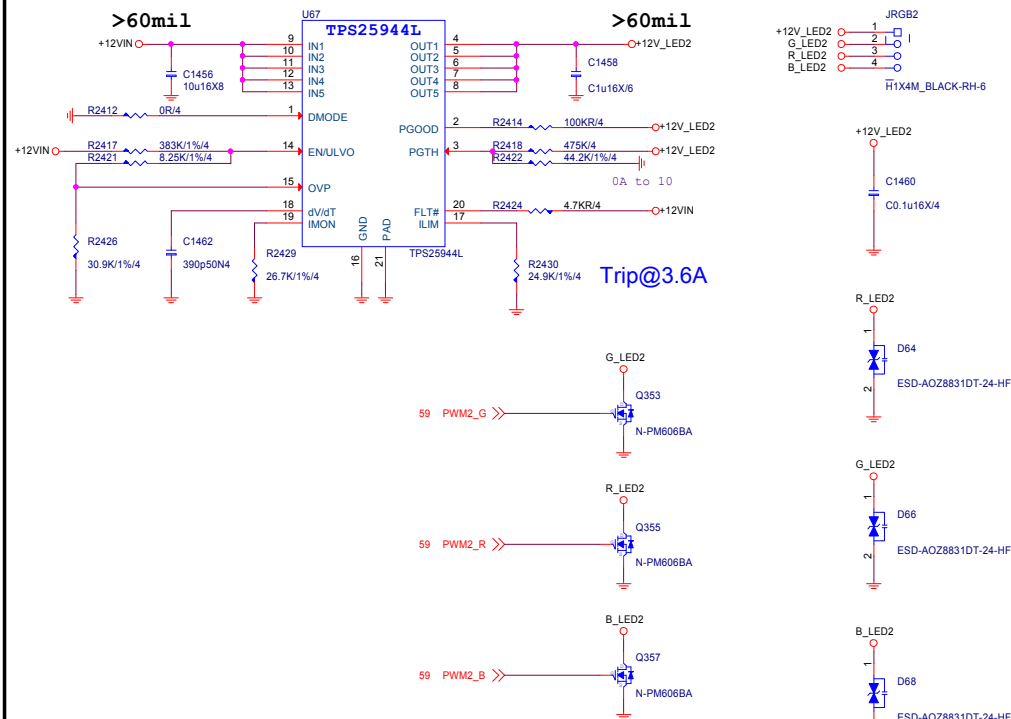


Control	Net Name	PWM USE
FCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

[illegible][illegible][illegible][illegible][illegible]

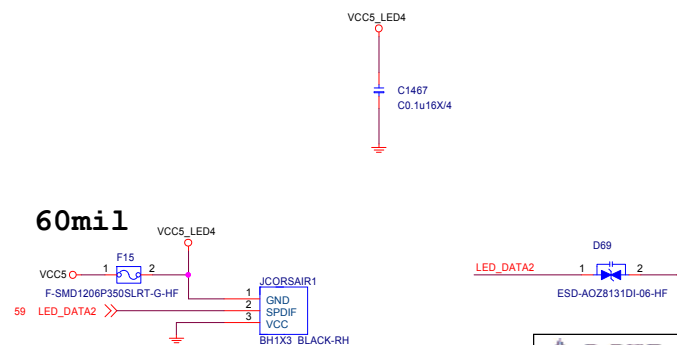
JRGB1

外接LED 燈條 (RGB )  
 ---- PCB 文字面 (JRGB1)  
 ---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

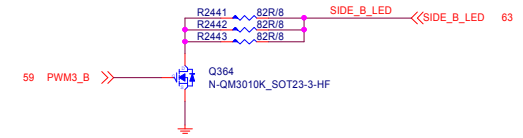
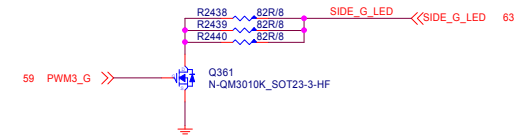
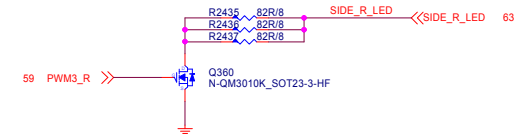
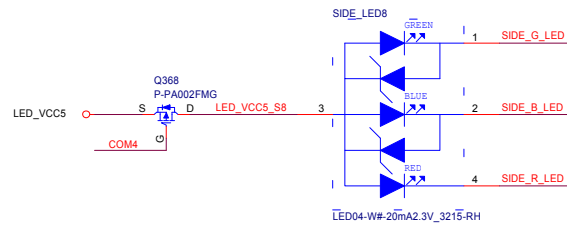
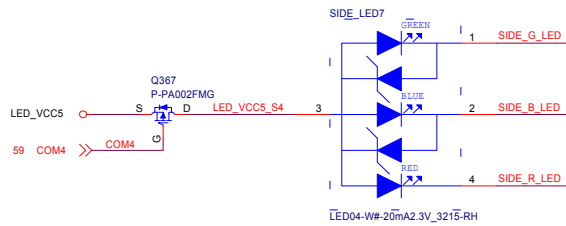
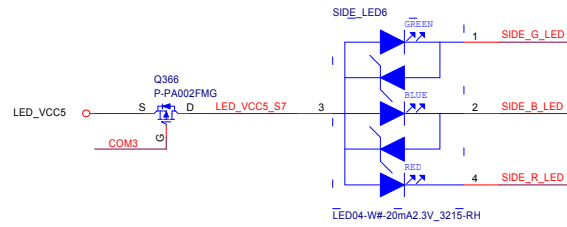
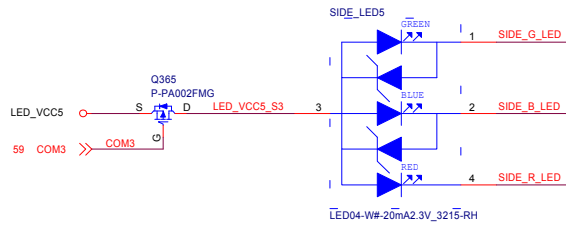
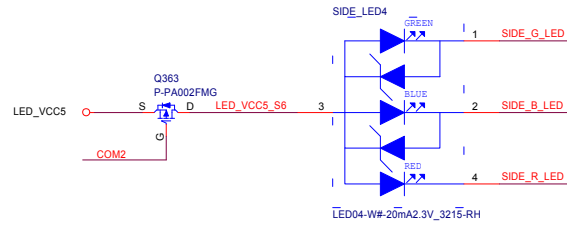
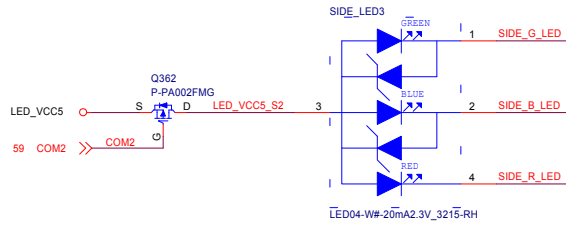
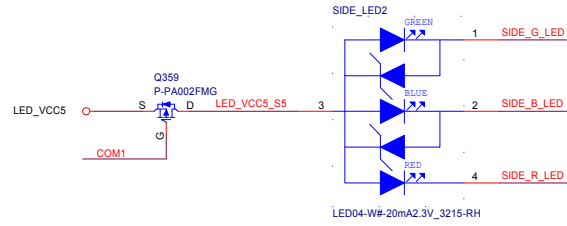
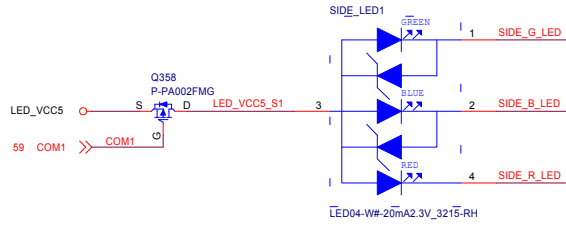
JRAINBOW1JRGB2

外接LED 燈條 (RGB )  
 ---- PCB 文字面 (JRGB2)  
 ---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

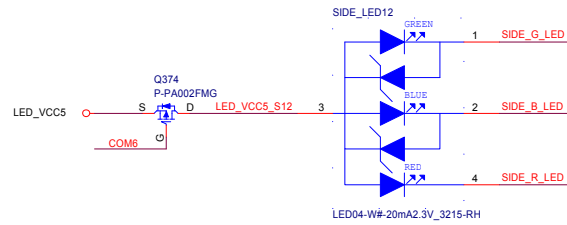
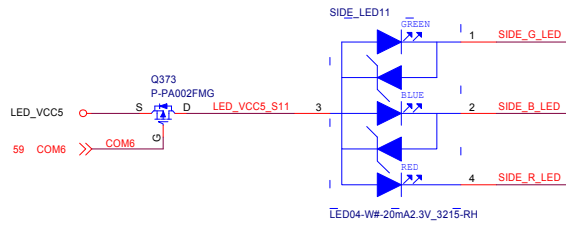
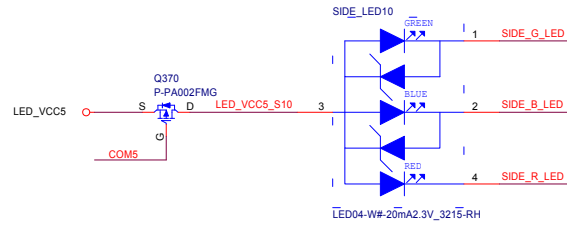
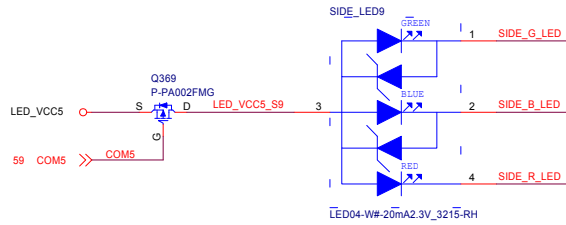
JCORSAIR1



# BOARD SIDE LED \*8

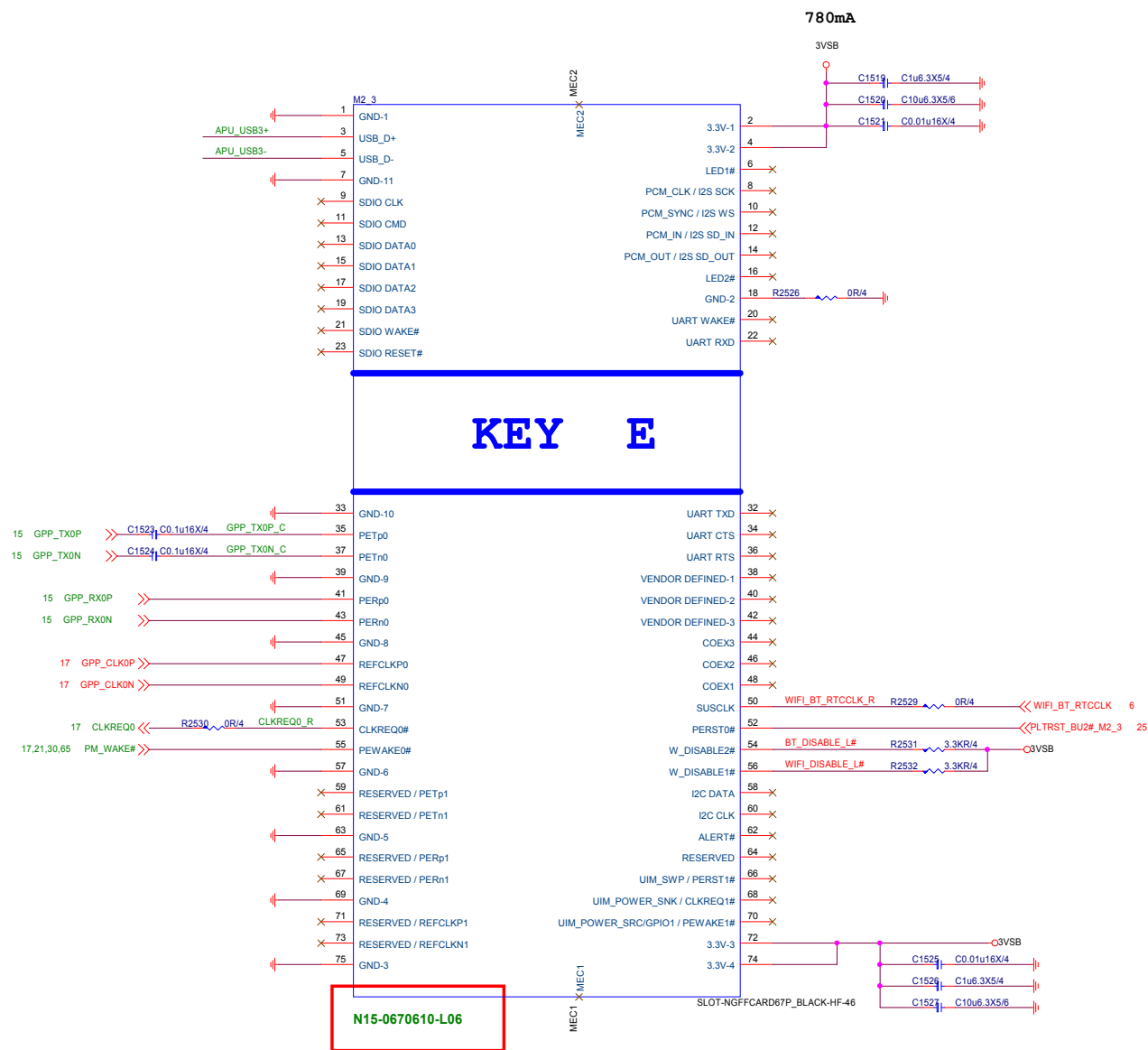
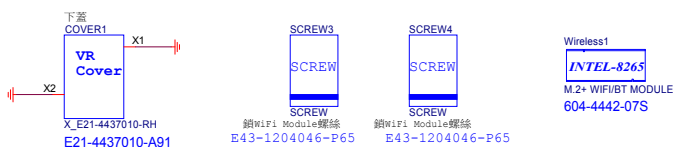


# FCH SIDE LED \*4



SIDE\_G\_LED << SIDE\_G\_LED 62  
 SIDE\_B\_LED << SIDE\_B\_LED 62  
 SIDE\_R\_LED << SIDE\_R\_LED 62

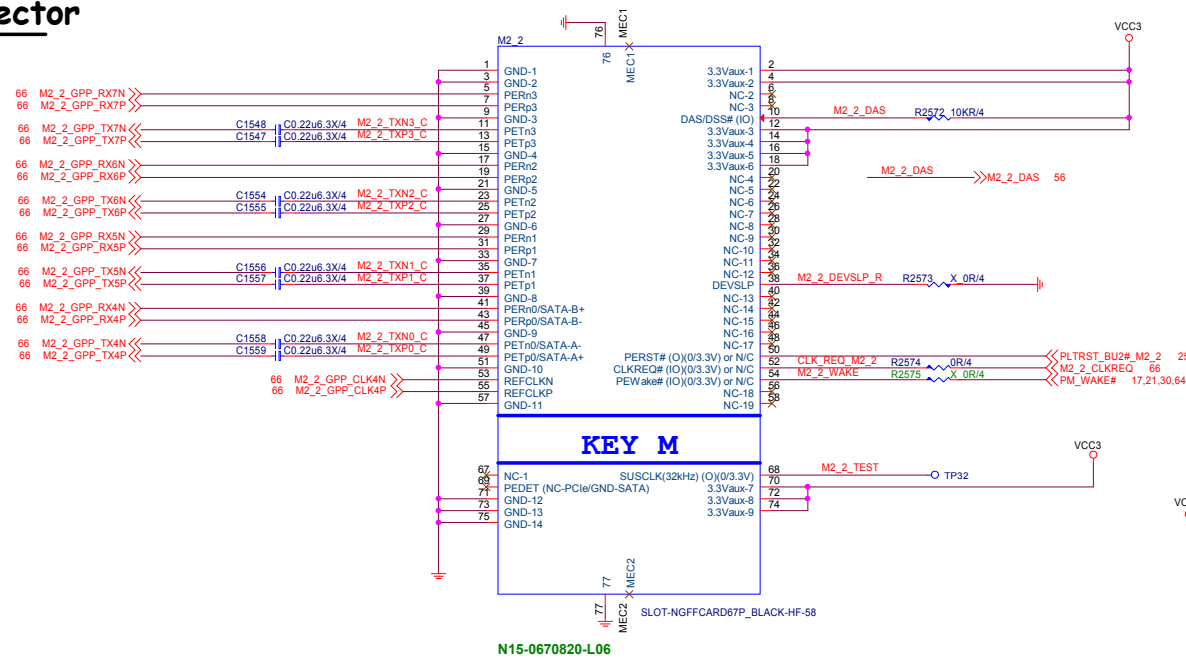




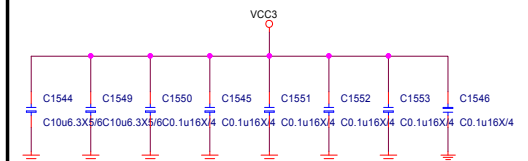
10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V3V pins 2 and 4.  
10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V3V pins 70 and 72.

## M.2\_2 Connector

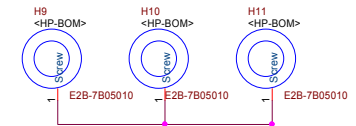
3.3V@2.5A



3.3V@2.5A



E2B-7984020-A89 E43-1203516-A89



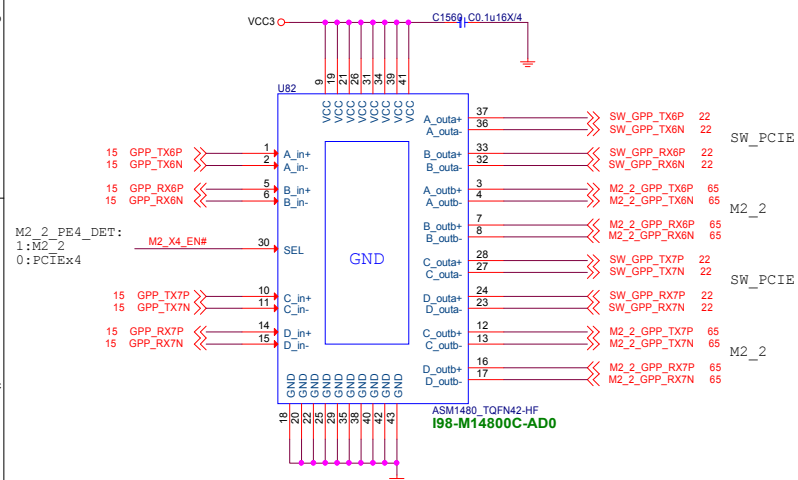
Footprint: H\_R240D173\_BR189\_PT

E2B-7B05010-A89 E2B-7B05010-A89  
E2B-7B05010-A89

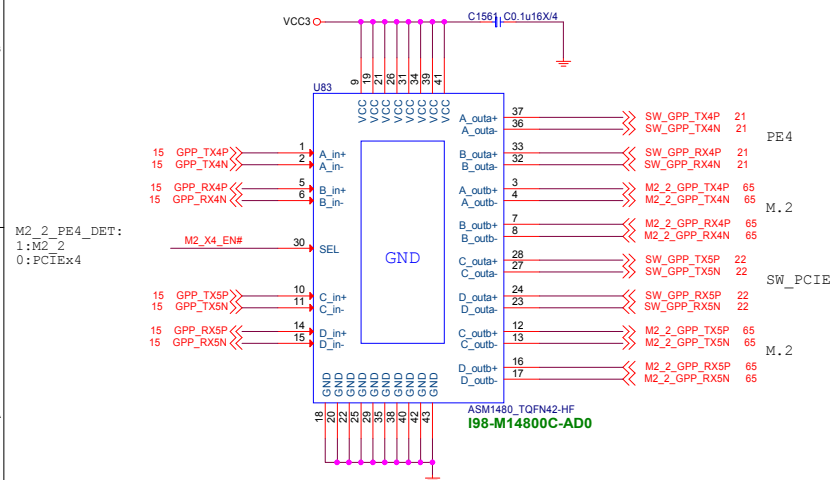
Schematic Cfg		Project	
CFG-7B85-10-Performance Gaming		V	A
CFG-7B85-20-Arsenal Gaming			

MSI MICRO-START INT'L CO.,LTD.			
Title: M.2_2			
Size: Custom	Document Number: MS-7B85	Rev: 11	
Date: Friday, June 29, 2018	Sheet: 65	of 75	

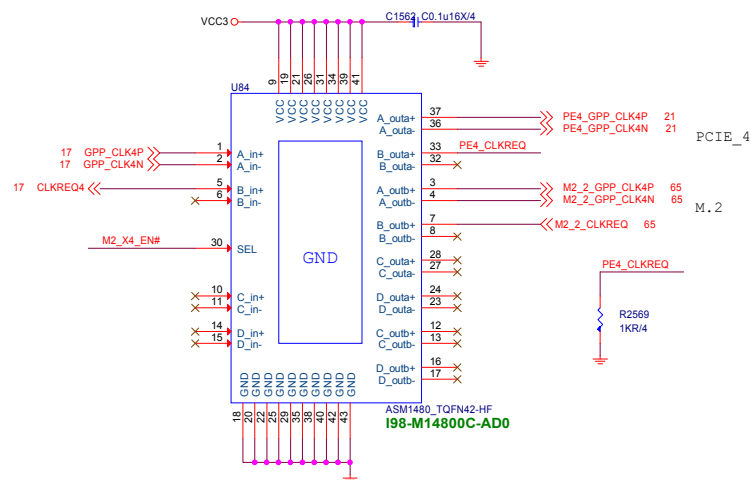
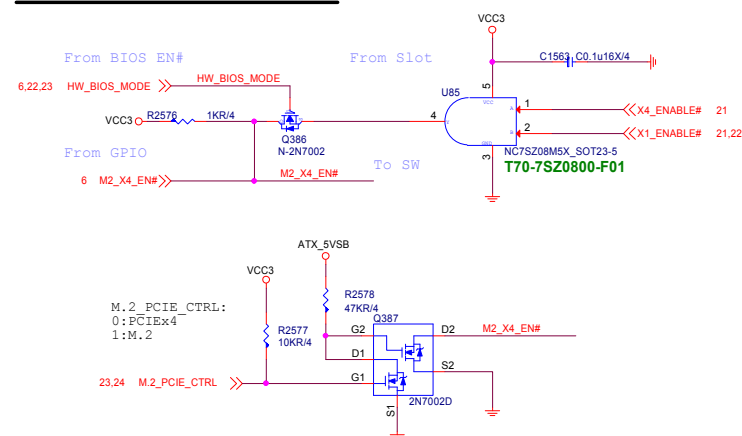
M2 2 and PCI E4 Switch



SEL	Function
L	N_in +/1 to N_outa+/-
H	N_in +/1 to N_outb+/-



### PCIE Lanes control circuit



# OPTION BOM PARTS

## 60 Level

	A	B	C	D	E
PCIE X16 SLOTT	OPT_PCIE_X16_1 [REDACTED] SLOT_PCIEXP164_13 N11-1641491-L06	OPT_PCIE_X16_2 [REDACTED] SLOT_PCIEXP164_13 N11-1641671-L06			OPT_PCIE_X16_3 [REDACTED] SLOT_PCIEXP164_13 N11-1641671-L06
PCIE X8 SLOTT	OPT_PCIE_X8_1 [REDACTED] SLOT_PCIEXP100_5 N11-1000221-L06	OPT_PCIE_X8_2 [REDACTED] SLOT_PCIEXP100_3 N11-1000261-L06	OPT_PCIE_X8_3 [REDACTED] SLOT_PCIEXP100_5 N11-1000221-L06	OPT_PCIE_X8_4 [REDACTED] SLOT_PCIEXP100_3 N11-1000231-L06	OPT_PCIE_X8_5 [REDACTED] SLOT_PCIEXP100_5 N11-1000261-L06 FOOTPRINT SLOT_PCIEXP100_5 可包容 SLOT_PCIEXP100_3
REAL USB Type A	OPT_USBA_1 [REDACTED] USB_A1_9_USB3_1_1 N53-09M0861-L06	OPT_USBA_2 [REDACTED] USB_A1_9_USB3_1_1 N53-09M0591-L06	OPT_USBA_3 [REDACTED] USB_A1_9_USB3_1_1 N53-09M0671-L06	OPT_USBA_4 [REDACTED] USB_A1_9_USB3_1_1 N53-09M0851-L06	OPT_USBA_5 [REDACTED] USB_A1_9_USB3_1_1 N53-09M0851-L06
SOLID CAP 270u16	OPT_270u16_BLK1 [REDACTED] C_P3_5_D8_H8 C71-2711761-N07	OPT_270u16_GLD1 [REDACTED] C_P3_5_D8_H8 C71-2711771-N07			FOOTPRINT C_P3_5_D8_H12 因為機構無法使用 請注意! C_P3_5_D8_H9 可包容 C_P3_5_D8_H8
SOLID CAP 560u6.3	OPT_560u6.3_BLK1 [REDACTED] C_P2_5_D6_3_H9_5 C71-5610671-N07	OPT_560u6.3_GLD1 [REDACTED] C_P2_5_D6_3_H9_5 C71-5610671-N07			FOOTPRINT C_P2_5_D6_3_H9_5 可包容 C_P2_5_D6_3_H9
SOLID CAP 470u6.3	OPT_470u6.3_BLK1 [REDACTED] C_P2_5_D6_3_H9_5 C71-4710671-N07	OPT_470u6.3_BU1 [REDACTED] C_P2_5_D6_3_H9 C71-4710671-A05			FOOTPRINT C_P2_5_D6_3_H9_5 可包容 C_P2_5_D6_3_H9
SOLID CAP 100u16	OPT_100u16_BLK1 [REDACTED] C_P2_5_D6_3_H5 C71-1011611-N07	OPT_100u16_GLD1 [REDACTED] C_P2_5_D6_3_H5 C71-1011611-N07			FOOTPRINT C_P2_5_D6_3_H5 可包容 C_P2_5_D6_3_H5
MEM SLOTT	OPT_MEM_BLK1 [REDACTED] DDRIV_D288 N13-2880581-L06	OPT_MEM_RED1 [REDACTED] DDRIV_D288 N13-2880701-L06			OPT_MEM_WHITE1 [REDACTED] DDRIV_D288 N13-2880541-L06 FOOTPRINT DDRIV_D288 1_2 可包容 DDRIV_D288
MKT6 Label	OPT_X370_1 [REDACTED] X370 KRAIT GAMING G51-M1SPK85-Q13	OPT_B450_1 [REDACTED] B450 GAMING PRO CARBON ACX370 SLI PLUS G51-M1SPN07-Q13	OPT_X370_2 [REDACTED] G51-M1SPK87-Q13	OPT_X470_1 [REDACTED] X470 GAMING PRO G51-M1SPM51-Q13	OPT_X470_4 [REDACTED] X470 GAMING PLUS G51-M1SPM54-Q13
PCH SINK	OPT_PCH_SINK_1 [REDACTED] AURAS E31-0409730-A87	OPT_PCH_SINK_2 [REDACTED] X470 GAMING PLUS E31-0409460-K08	OPT_PCH_SINK_3 [REDACTED] HS-0408800-RH E31-0408920-K08	OPT_PCH_SINK_4 [REDACTED] KRAIT E31-0408970-A87	
MOSN +IO	OPT_MOSN_IO_1 [REDACTED] AURAS E31-0505750-A87	OPT_MOSN_IO_2 [REDACTED] SLI PLUS E31-0505420-K08	OPT_MOSN_IO_3 [REDACTED] KRAIT E31-0504780-K08	OPT_MOSN_IO_4 [REDACTED] PRO E31-0504820-A87	
MOSW	OPT_MOSW_1 [REDACTED] AURAS E31-0505740-A87	OPT_MOSW_2 [REDACTED] SLI PLUS E31-0505430-K08	OPT_MOSW_3 [REDACTED] KRAIT E31-0504790-K08	OPT_MOSW_4 [REDACTED] PRO E31-0504830-A87	
PS2_USB	OPT_PS2_USB_1 [REDACTED] IOASM_USB_DIN14 N58-14M0211-F02	OPT_PS2_USB_2 [REDACTED] MINIDIN_USBX2-RH-10 N58-14M0241-H06			
HDMI_USB	OPT_HDMI_USB_1 [REDACTED] IOASM_USB3_HDMI37 N58-37M0101-L06	OPT_HDMI_USB_2 [REDACTED] IOASM_USB3_HDMI37 N58-37M0111-L06			
LAN_USB	OPT_LAN_USB_1 [REDACTED] IOASM_RJ45_USB_LED32 N58-32F0291-F02	OPT_LAN_USB_2 [REDACTED] RJ45_USBX2_LEDX2-1000-RH N58-32F0311-F02			

## 5010 Level

	A	B	C	D	E
FCH	OPT_X470_NB [REDACTED] PROM_B450 OB1-7B78001-A08	OPT_B450_NB [REDACTED] 218-0831005-00-RH B01-21808L5-A08			
M.2 SLOTT	OPT_M2_1 [REDACTED] SLOT_NGFFCARD67_31 N15-0670820-L06	OPT_M2_2 [REDACTED] SLOT_NGFFCARD67_2 N15-0670330-L06	OPT_M2_3 [REDACTED] SLOT_NGFFCARD67_33 N15-0670810-L06		FOOTPRINT SLOT_NGFFCARD67_31 可包容 SLOT_NGFFCARD67_2
REAL USB Type C	OPT_USBC_1 [REDACTED] USB_C1_24_2 N53-24M0180-L06	OPT_USBC_2 [REDACTED] USB_C1_24_2 N53-24M0040-L06			
PCB	OPT_PCB_1 [REDACTED] 7885-11 PD0-07B8511-G37 PD0-07B850A-E48	OPT_PCB_2 [REDACTED] 7A33-21 PD0-07A3321-G37 PD0-07A3321-E48	OPT_PCB_3 [REDACTED] 7A33-31 PD0-07A3331-G37 PD0-07A3331-E48		
0 Ohm (0402)	OPT_0OHM_5010_1 [REDACTED] UR24 5010_0402 R11-0000012-W08				
LED	OPT_LED_RED_5010_1 [REDACTED] LED04-R-20mA2.4V_1608-HF D0C-040P100-H91				

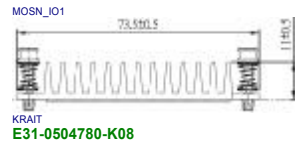
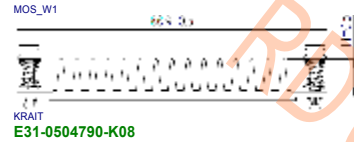
## 5020 Level

	A	B	C	D	E
LED	OPT_LED_LED_5020_1 [REDACTED] LED04-BR-25mA2.35V_1711-RH 5020_0402 D0C-040S600-E07				

## 60 Level

	A	B	C	D	E
Audio cover	OPT_AUD_COV_1 [REDACTED] AUDIO_COVER_20X19_5 E21-7A59010-A91				OPT_AUD_COV_2 [REDACTED] AUDIO_COVER_20X19_5 E21-7A62010-A91
Audio Jack	OPT_AUD_JACK_1 [REDACTED] JACK_AUD_D26P N54-26F0351-L06				OPT_AUD_JACK_2 [REDACTED] JACK_AUD_D26P_U2 N54-26F0361-L06
M.2 SCREW	OPT_M2_SCR_1 [REDACTED] SCREW E2B-7A69010-A89				
PCIE X4 SLOTT	OPT_PCIE_X4_1 [REDACTED] SLOT_PCIEXP100_5 N11-1000221-L06	OPT_PCIE_X4_2 [REDACTED] SLOT_PCIEXP100_5 N11-1000261-L06			

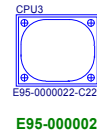
## MOS SINK



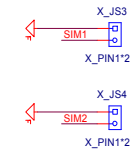
## DDR Cover

11-16  
RM: E95-0000022-C22/ E95-0000022-A91

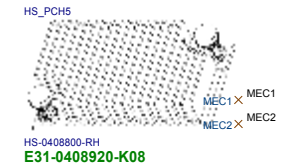
## CPU Socket



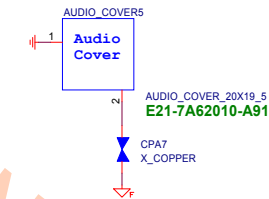
## Simulation



## PCH SINK



## AUDIO COVER



## MANUAL PART



AVL:  
D06-0100161-P52  
D06-0100101-K26



7B85-0A  
PD0-07A340A-G37, 精成-深圳, 23, 寶安恩斯通廠 (MSIS)  
PD0-07A340A-E48, 騰華, 23, 寶安恩斯通廠 (MSIS)

## BIOS LABEL



## MKTG name Label



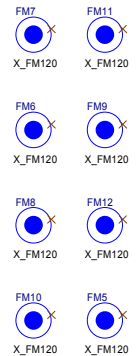
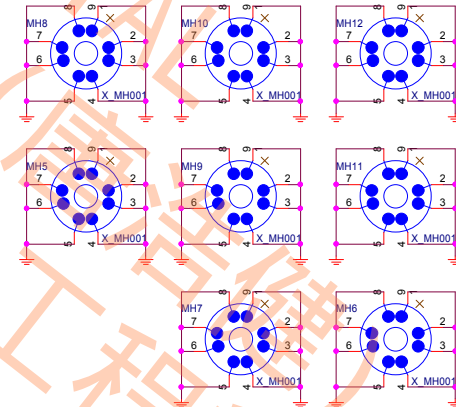
## ROYALTY



cFosSoftware GAMING Only



## Optics Orientation Holes



Schematic Cfg		Project	
CFG-7B85-10-Performance Gaming		V	A
CFG-7B85-20-Arsenal Gaming			

MSI MICRO-START INT'L CO.,LTD.			
Manual Parts			
File			
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